Vol. 50 • No. 4

April 2007

Microwave Journal

Amplifiers and Oscillators

Amplifiers and Oscillators: The Landscape in 2007

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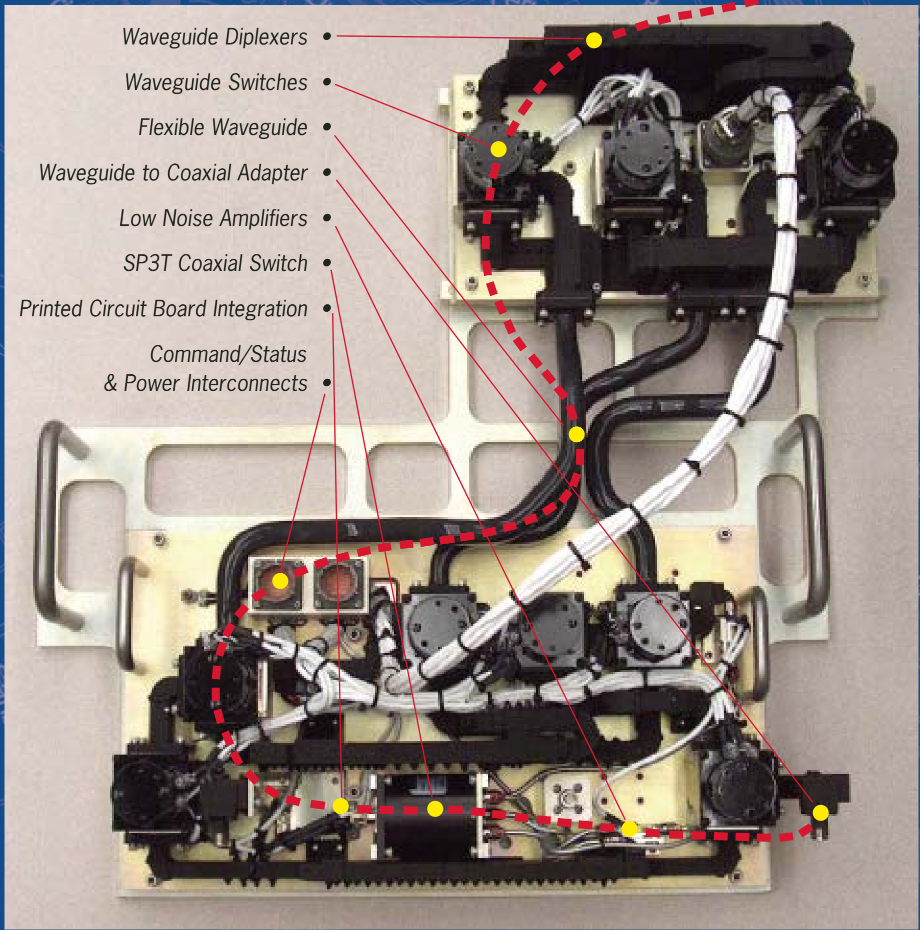

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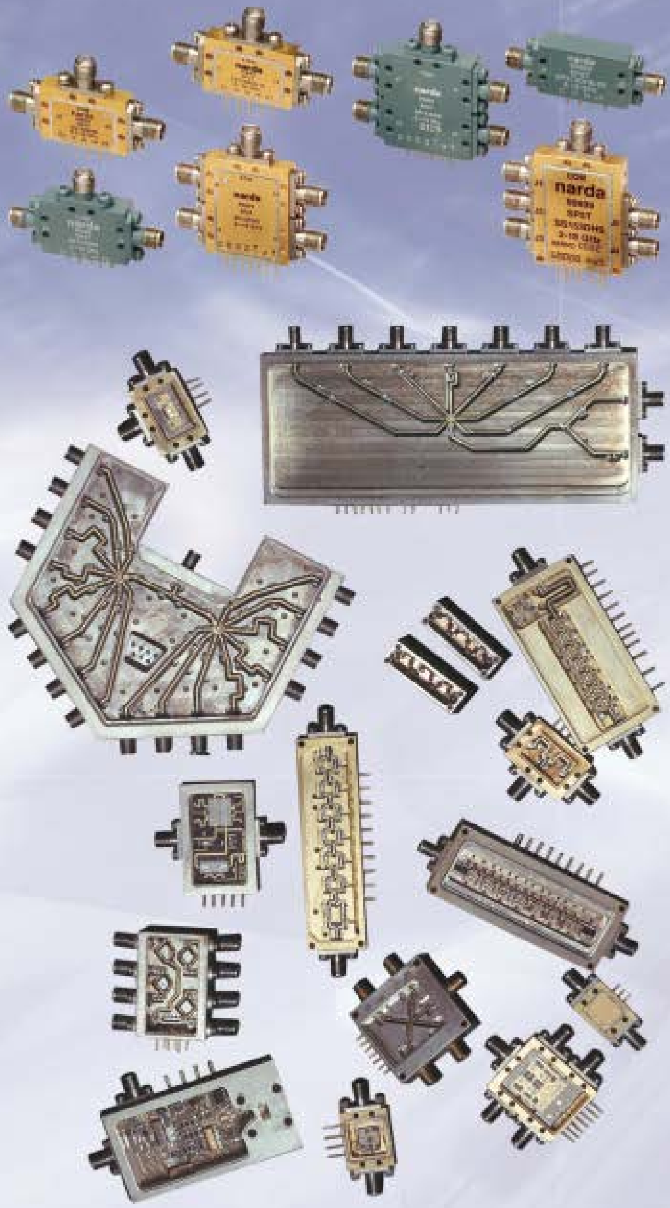

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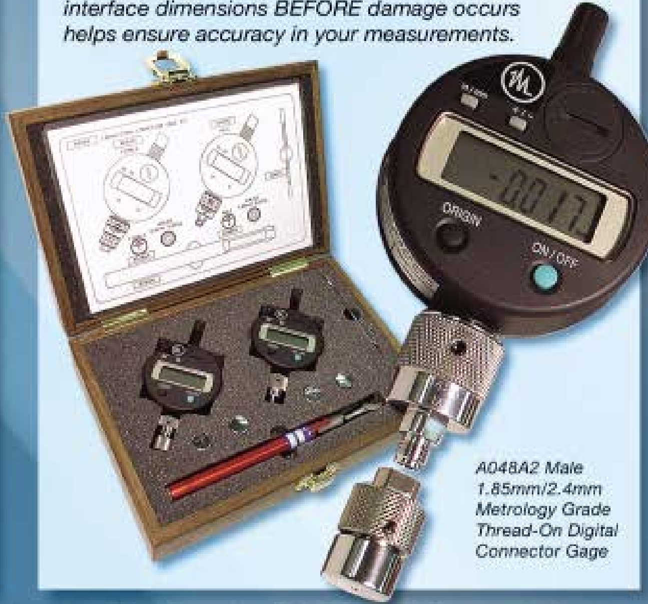

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FEATURES

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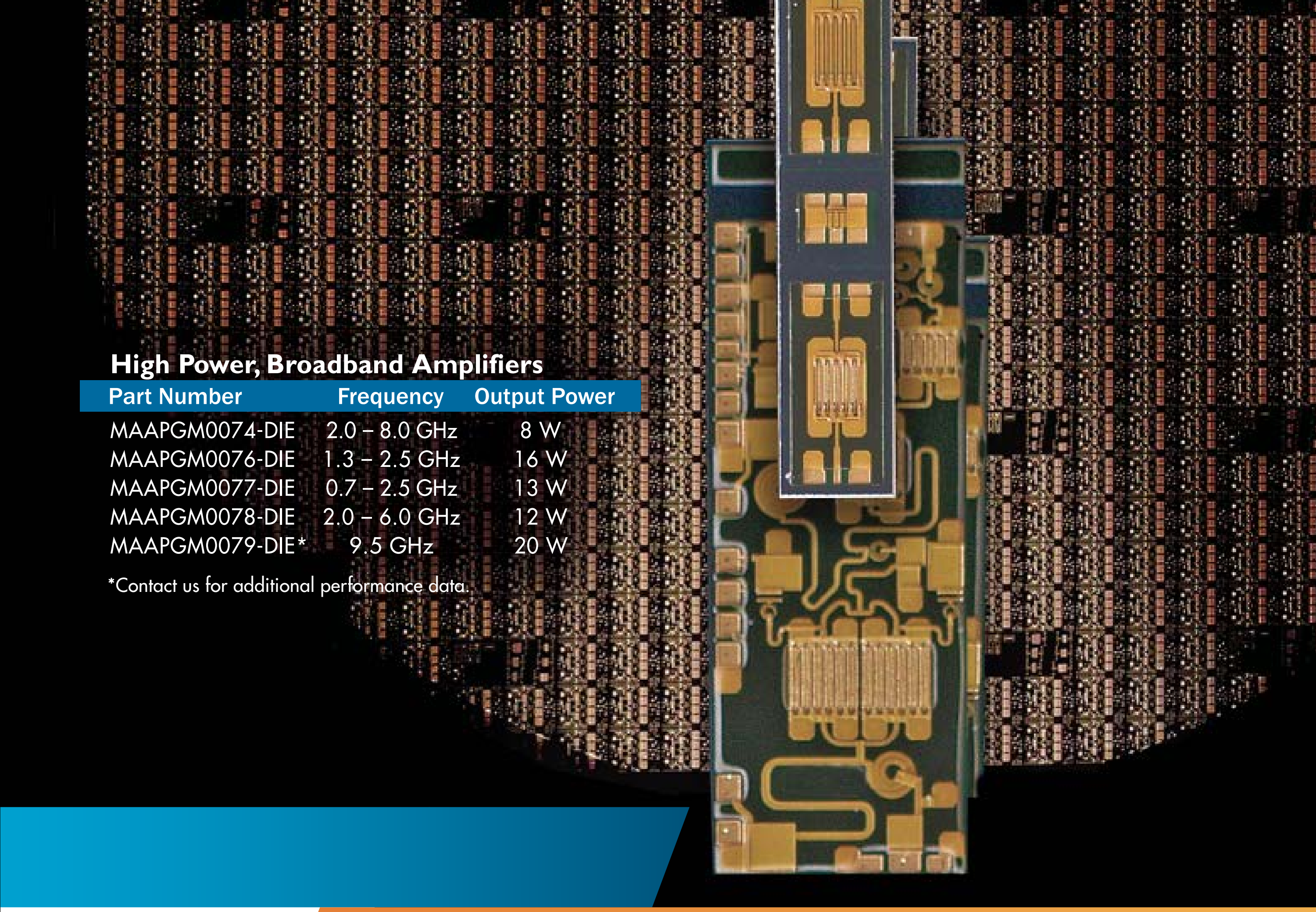

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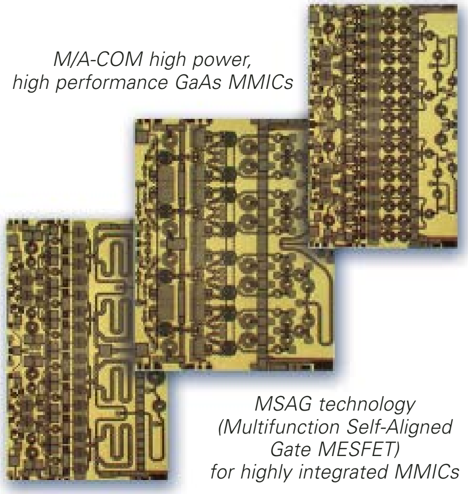

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Microwave Journal

FEATURES

DEPARTMENTS

Cover design by Igor Valdman

THIS MONTH ON THE WEB

Visit www.mwjournal.com for the latest industry news and exclusive on-line articles

RF&HYPER EUROPE 2007

RF & Hyper Europe 2007
March 27–29, 2007
CNIT-Paris la Defense

Richard Mumford, *Microwave Journal*'s European Editor, provides a wrap-up of select news, information and product announcements at this year's RF & Hyper show, including a detailed look at the new products on display.

Lean Manufacturing

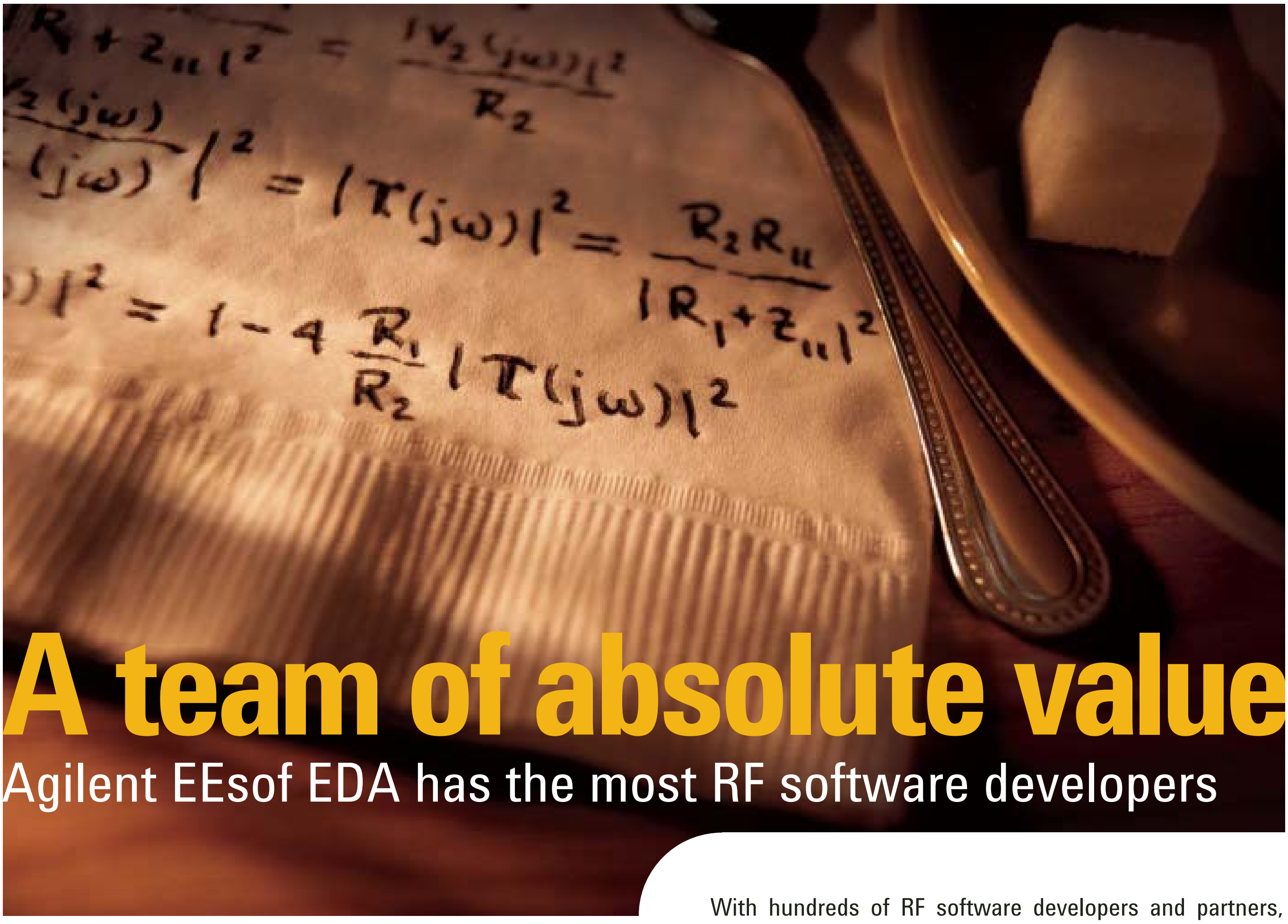
UltraSource Inc.

While much of the microelectronics world is struggling to figure out if Lean Manufacturing is achievable in their facilities, one thin film electronics supplier has embraced it whole-heartedly—and in the process has already increased daily production rates on its main production line by 475%. The lessons learned are ready to be explored and documented for companies who are struggling with adopting this idea at the microelectronics level.

Microwave Journal **Buyer's Guide**

Product Focus: Amplifiers and Oscillators

In conjunction with this month's editorial theme, we've compiled a complete listing of amplifier and oscillator products currently featured in our on-line Buyer's Guide. The *Microwave Journal* on-line Buyer's Guide is the RF/microwave engineers' complete source for products and services featuring over 1000 companies.



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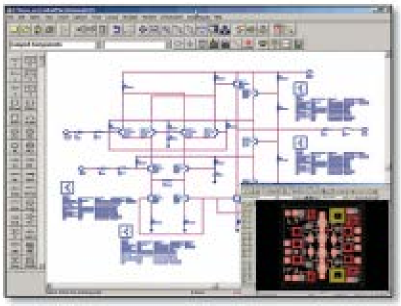

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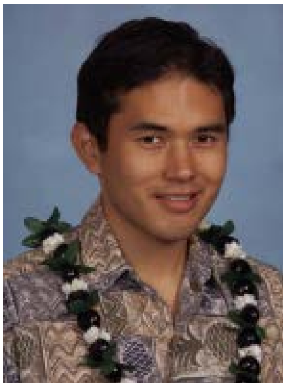
IMS 2007: GUEST TOUR PROGRAM



Hawaii's unique location in the middle of the vast Pacific Ocean has created an environment that is home to a distinctive blend of sights, sounds and cultures. Its warm, clean blue waters, awe-inspiring volcanic eruptions, and fusion of Asian/Pacific/Western customs have captured the hearts of both visitors and residents alike. As a kama'aina (person born and raised in Hawaii), these islands have a special place in my heart, and I have always loved playing the role of tour guide with friends and family that come to visit. As such, I am very excited to present to you the IMS 2007 guest tours.

After months of careful planning, I believe the Steering Committee and I have chosen an exciting array of 12 guest tour programs, allowing you to marvel at the destruction of molten lava flows, taste the melt-in-your-mouth feel of an ancient Hawaiian-style imu roasted pig, travel across the varied cultures of the South Pacific through song and dance, or relax on a romantic dinner cruise while admiring the beautiful Waikiki skyline.

Since we know that Hawaii cannot be captured in 12 simple tours, we have also arranged for additional tours that can be booked any day of the week, offering a little flexibility for our attendees during the conference. And for those that would like to plan an outer-island getaway before or after the conference, as many visitors to Hawaii do, we have arranged three-night rental car and hotel packages for your convenience.

A full list of guest tours and outer-island packages can be viewed at www.mcahawaii.com/grps07/ims2007hi. The advance registration deadline for all recreational activities is May 15, but for those that miss this deadline, a desk will be set up at the Hawaii Convention Center and both Hospitality Suites during the convention. We strongly encourage advance registration, however, due to the limited number of openings for some tours.

All in all, I believe you will see that there is a wide assortment of tours for both children and adults to choose from, and I invite all IMS 2007 attendees to invite family and friends to share in this wonderful opportunity. I hope to see you in June! ■

KENDALL S. CHING
Guest Program Chair, IMS 2007

Ask Harlan

How it works: Harlan has selected one question from his "Ask Harlan" column to be featured in the magazine. Please visit www.mwjournal.com/askharlan to provide an answer to this month's featured question (see below). Harlan will be monitoring the responses and will ultimately choose the best answer to the question. Although all of the responses to the featured question will be posted on our web site, we plan to publish the winning answer in the June issue. All responses must be submitted by **May 4, 2007**, to be eligible for the participation of the April question.

The winning response will win a free book from Artech House, along with an "I Asked Harlan!" t-shirt. In addition, everyone who submits a legitimate response will be sent an "I Asked Harlan!" t-shirt.

February Question and Winning Response

The February question was submitted by Peter Saul from Saul Research:

Dear Harlan,

What happened to the "Hula Hoop" antenna, AKA DDRR? It was reported in the 1960s, but not since. It appears from the references (*Microwave Journal*, Vol. 6, No. 11, November 1963, pp. 89–90; how can I get a copy?) to have had lots of promise.

The winning response to the February question is from Randy Williams of SunShine Electronic Repair:

I have found that the "Hula Hoop" antenna is alive and is researched by different people including a physicist. Mobile communications applications for handsets was one use of the Hula Hoop antenna. The DDRR, invented by Dr. Boyer from Northrop, is used for military applications on warships. Dr. Boyer published an article that included technical information and a mathematical formulation of DDRR based on transmission line theory. Entitled "Suprising Miniature Low Band Antenna," the article should be easy to find through research. The antenna had a very low impedance, very selective, low noise antenna responding to the magnetic component of the radio wave, low angle, tunable, very high Q. Below is where you can find the article on Dr. Boyer and where to purchase a publication that expands on the Hula Hoop antenna and mobile communication. VE2DLJ and VE2AMT found some ten years ago an old copy of the 73 magazine articles and decided to build a prototype. They contacted Dr. Boyer and have had numerous discussions with him. He warned them and told them "not to cut corners." His recommendations included: use big tubing (four inches or more for 75 m); do not use automotive exhaust pipe (it will rust and contact losses will transform the antenna into a dummy load); all contacts and connections must be A1; solder corners, if you make it square, use Penetrox everywhere; use very high voltage vacuum capacitors and high quality isolators to support the rings; do not use chicken wire. Dr. Boyer was horrified by some description of DDRRs using chicken wire. He explained that measurements made by Northrop engineers showed that the near field is in concentric rings on a one ring DDRR and that chicken wire could add losses. For the complete article, go to: http://www.orionmicro.com/ant/ddrr/ddrr1.htm. Also look for a publication called *HandBook of Antennas in Wireless Communications*.

This Month's Question of the Month

(answer on-line at www.mwjournal.com/askharlan)

Satyajit Chakrabarti from SAMEER Kolkata Centre has submitted this month's question:

How can a single antenna be made to operate at three or four frequencies? Is there any bandwidth limitation?

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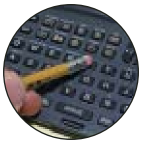

Coming Events

CALL FOR PAPERS

Antenna Measurement Techniques Association (AMTA 2007)
by May 7, 2007
Asia-Pacific Microwave Conference (APMC 2007)
by June 15, 2007

APRIL

IEEE Radar Conference
April 17–20, 2007 • Waltham, MA
www.radar2007.org

JUNE

IEEE MTT-S International Microwave Symposium
June 3–8, 2007 • Honolulu, HI
www.ims2007.org

IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2007)
June 3–8, 2007 • Honolulu, HI
www.rfic2007.org

69th ARFTG Conference
June 7–8, 2007 • Honolulu, HI
www.arftg.org

IEEE International Symposium on Antennas and Propagation (AP-S)
June 10–15, 2007 • Honolulu, HI
http://hcac.hawaii.edu/conferences/aps2007/

WCA 2007
June 12–15, 2007 • Washington, DC
www.wcai.com/events.htm

4th International Workshop on Advanced Ground Penetrating Radar (IWAGPR 2007)
June 27–29, 2007 • Naples, Italy
www.irea.cnr.it/IWAGPR2007

JULY

IEEE EMC Symposium
July 8–13, 2007 • Honolulu, HI
www.emc2007.org

AUGUST

International Symposium on Antennas and Propagation (ISAP 2007)
August 22–24, 2007 • Niigata, Japan
www.isap07.org

SEPTEMBER

IEEE International Conference on Ultra-WideBand (ICUWB 2007)
September 24–26, 2007 • Singapore
www.icuwb2007.org

OCTOBER

European Microwave Week (EuMW 2007)
October 8–12, 2007 • Munich, Germany
www.eumweek.com

AOC International Symposium and Convention
October 28–31, 2007
Orlando, FL
www.crows.org

Military Communications Conference (MILCOM 2007)
October 29–31, 2007
Orlando, FL
www.milcom.org

NOVEMBER

Antenna Measurement Techniques Association (AMTA 2007)
November 4–9, 2007 • St. Louis, MO
www.amta2007.com

DECEMBER

Asia-Pacific Microwave Conference (APMC 2007)
December 11–14, 2007 • Bangkok, Thailand
www.apmc2007.org

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Workshops & Courses

Reverberation Chamber Theory and Experiment Short Course

■ **Topics:** This course is designed for engineers who will be involved in radiated emission or immunity testing of commercial or military systems using reverberation chambers. The theory portion will cover the statistical nature of reverberation chamber testing, characterization of the EM test conditions, and the tradeoff between uncertainty in test results and test time. The experiments include typical measurement techniques, chamber calibration, immunity, emission and pulse testing in reverberation chambers.
■ **Site:** Stillwater, OK
■ **Dates:** April 30–May 4, 2007
■ **Contact:** For more information, visit http://rc-course.okstate.edu.

2007 IEEE Microwave Theory and Technique (MTT) Short Course

■ **Topics:** "Power the Future" is a short course with leading researchers and distinguished professors. The course will cover WLAN, WiMAX, cellular and emerging 60 GHz+ applications.
■ **Site:** Menlo Park, CA
■ **Date:** May 5, 2007
■ **Contact:** For more information, visit www.mtt-scv.org.

Making Accurate Low Level Electrical Measurements

■ **Topics:** This course provides users with a detailed understanding of how to make accurate low level electrical measurements. Users will learn what constitutes a low level measurement, the limitations of these measurements, sources of measurement error and techniques to eliminate these errors. Additional topics include selecting the proper product for a desired measurement and understanding the basics of how to communicate with an instrument from a PC. The session consists of lectures, demonstrations and hands-on labs.
■ **Site:** Cleveland, OH
■ **Dates:** June 19–20, 2007
■ **Contact:** For more information, visit www.keithley.com.

Practical Antenna Design

■ **Topics:** The course covers the important and timely issues involving modern antenna design and theory. Developed specifically for engineers and designers who work with radar and radio communications, this workshop will give participants the understanding of antenna theory and techniques, the skills to analyze, design and measure various antennas, and the knowledge of antenna measurements. For more information, visit www.conted.ox.ac.uk.
■ **Site:** Summertown, Oxford, UK
■ **Dates:** June 20–21, 2007
■ **Contact:** University of Oxford Continuing Education, +44 (0) 1865 286958 or e-mail: electronics@conted.ox.ac.uk.

The Entrepreneurial Engineer

■ **Topics:** This short course is an efficient and memorable introduction to the personal, interpersonal, business and organizational skills necessary to help engineers of applied science and mathematics perform at high levels in today's increasingly opportunistic organizations and enterprises. For more information, visit http://online.engr.uiuc.edu/shortcourses/tee/index.html.
■ **Site:** Archived on-line course.
■ **Dates:** Archived on-line for anytime viewing.
■ **Contact:** University of Illinois at Urbana-Champaign, 117 Transportation Bldg., 104 S. Mathews Avenue, Urbana, IL 61801 (217) 333-0897 or e-mail: deg@uiuc.edu.

PCB Design Techniques for EMC and Signal Integrity

■ **Topics:** This course will assist practicing engineers who are responsible for PCB designs and system-level products. Disciplines include PCB layout, logic design, regulatory compliance and EMC. For more information, visit http://epdwww.engr.wisc.edu.
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COVER FEATURE
INVITED PAPER

AMPLIFIERS AND OSCILLATORS: THE LANDSCAPE IN 2007

A dozen years ago, it crossed my mind that Winslow Homer's dramatic (some would say melodramatic) painting, "The Gulf Stream" (see ***Figure 1***), was a nearly perfect metaphor for the microwave industry. The ship of microwave industry is foundering in the turbulent, tropical water, afloat but with the mast snapped off and rudder missing; the poor engineer is still supported by that industry, but it is unclear how long that will continue; the sharks of unemployment are circling; the only hope of rescue, wireless technology, is almost invisible in the distance; and, finally, the economic waterspout, which caused all the damage, is leaning ominously toward that rescuer. Was there any hope? Indeed, there was. Wireless technology has taken hold more strongly than most of us would have predicted, and has replaced a lot of volatile military business with more stable commercial business, motivated by a genuine demand from the public instead of the mercurial interests of politicians. Still, that technology has presented challenges that are startlingly difficult to meet, and they have changed the face of amplifier and oscillator design dramatically. Many of us, accustomed to heavily funded, ultra-high tech aerospace industries, were tempted to think that commercial electronic design would not be particularly challenging. Those of us beset by that illusion have been humbled, indeed.

Fig. 1 Winslow Homer's "The Gulf Stream"—a metaphor for the wireless industry?

I thought it might be fun to look at some of these technologies and see how they have affected amplifier and oscillator design, how

STEVE MAAS
Applied Wave Research Inc.
El Segundo, CA

they have created new demands, and how well those demands are being met. As it happens, I think we are doing pretty well. Certainly, challenges remain, and most of us would not have it any other way. This is one of those times when it is genuinely fun to be an engineer.

POWER AMPLIFIERS

Nowhere has the microwave landscape been changed more profoundly than in the area of power amplifier (PA) design. Not long ago, a solid-state PA with approximately 45 percent efficiency was considered quite a nice thing to have, even for such traditional high efficiency applications as spacecraft. Today, even for high linearity applications, that efficiency is marginal, and for applications where linearity is not needed (such as GSM cellular handsets), totally unacceptable. Efficiency alone is rarely enough; other requirements, such as size, cost and distortion, have assumed equal importance.

Power

Power really is not the problem. We can build amplifiers that provide any reasonable (or maybe even unreasonable) level of power that a user decides he must have. The real problem is to generate the required power consistent with all the other requirements placed upon the poor, suffering little PA chip. The most difficult of these are efficiency and linearity, directly opposing tradeoffs.

Efficiency

Obviously battery-powered equipment, such as cell phones and wireless network cards in laptop computers, must be efficient. The need for high efficiency is not limited to such applications, however. Efficiency is important even in cellular base stations, which seemingly have an inexhaustible supply of power. One reason is thermal management of the amplifiers and other equipment. A second reason, perhaps less obvious to the design engineer but painfully clear to the cellular operator, is the cost of electricity. A cellular base station can easily use $2500 worth of electricity per year; a large operator, who may have 40,000 such stations, pays $100M per year for electricity. As both energy prices and the number of base stations increase, this number has nowhere to go but up, as well as the air pollution and carbon emissions from the electrical generating stations needed to power them. As with other important power amplifier characteristics, efficiency intrinsically is not a problem. Amplifiers with power-added efficiencies well above 75 percent at cellular frequencies have been produced, even by this author, who claims no special expertise in the area, and efficiencies well into the 90 percent range regularly have been achieved, at low frequencies, by class-E amplifiers. The real problem is to achieve good efficiency along with other requirements, which often include linearity. Resolving these diametrically opposing tradeoffs is today's greatest challenge in power amplifier design.

Gain

At first glance, gain seems not to be very important. The higher the gain of the power stage, however, the smaller—and lower power—the driver stage needs to be. Viewing this another way, we might note that power-added efficiency increases as gain increases. This is important, as the gain of silicon devices is generally lower than that of GaAs heterojunction devices, so any move to the use of SiGe for handset power amplifiers will encounter this difficulty.[1]

Linearity

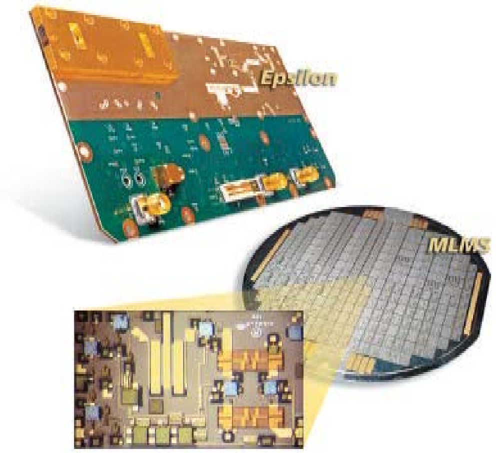
Linearity is probably the most difficult requirement to meet, not only because it is a direct tradeoff with other requirements, especially efficiency, but also because it is very difficult to identify the best approach to meeting it. It is indeed interesting to note that no theory of nonlinearity in large-signal circuits, similar to, say, Volterra-series theory in small-signal circuits, currently exists. Lack of such a theoretical basis makes modeling of devices and intuitive optimization of circuits a genuine dilemma. We know, for example, that much distortion of modulated signals is related to peak clipping, but what else? What parts of a transistor's I/V characteristic are most significant? What is the relative importance of resistive and capacitive nonlinearities? We generally assume that numerical simulation can answer such questions, but the results depend strongly on device models, and we need to answer those questions to model a device appropriately. Furthermore, numerical analysis of particular cases does not always provide the intuitive insight we need for a general understanding of design optimization. The best situation exists when numbers provide insight, and insight provides ideas that can be validated by numbers. As things stand, we are missing half that process.

Size and Cost

It seems that cell phones can never be small enough to satisfy consumers. Since the power amplifier is invariably a separate package from the rest of the digital and RF hardware, it consumes a disproportionate amount of space in the phone, in spite of its tiny package. Similarly, the cost of the power amplifier, although low, is still a significant part of the handset manufacturing cost. Any new technology that increases the size of the PA chip will be a hard sell to handset manufacturers. Technologies that require, say, quarter-wave transmission lines at 1800 MHz, are nonstarters for this application. Others, which employ digital signal processing (DSP) chips and, perhaps, modest improvements in size, might be better received, especially if they offer significantly increased efficiency. As Steve Cripps summarized it two years ago,[2] "Efficiency, power, linearity: pick any three." In the case of cellular PAs, I might increase the total to five by adding small size and low cost to the list.

APPROACHES TO PA DESIGN

Currently, the dominant method for achieving high efficiency, low distortion operation needed by cellular handsets is with class-AB, InGaP HBT amplifiers. These can have surprisingly good distortion characteristics, exhibiting adjacent-channel power ratios (ACPR) below –45 dBc with 40 to 45 percent efficiency. It is worthwhile to note that ideal class-B amplifiers do not produce odd-order intermodulation distortion (IMD). IMD, of which ACPR is a manifestation, probably arises primarily from peak clipping, nonlinear input/output characteristics and nonlinearity near the turn-on point of the devices. As we shall note, this evaluation of dis-



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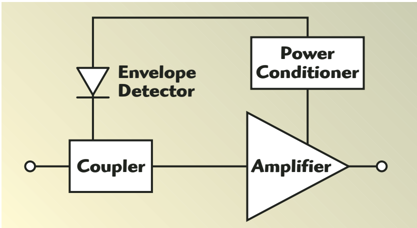
tortion sources is somewhat uncertain and necessarily incomplete, as a general theory of distortion in large-signal devices so far does not exist. An interesting question surrounds the possibility of using silicon technologies for handset power amplifier applications. The use of SiGe technology, in particular, could provide significant improvements in cost and integration. At present, some new capabilities are critically needed in silicon technologies before this can happen. An interesting invited paper at the 2007 SiRF Symposium explored some of the limitations.[1] Beyond the well recognized problem of low breakdown voltage, the author identified the need for through-wafer vias, thick gold or copper conductors (both to handle high current densities and to provide thermal uniformity), device and interconnect modeling, and thermal interaction in high density circuits as areas that must be addressed. It is remarkable to see that many old ideas for power amplifier design are currently being reevaluated. Many of these were well described by Cripps in his article two years ago, and in the recently published second edition of his classic text.[3] Many of these approaches are large, and thus are not likely ever to be used in handsets, although other applications are possible. One exception is the idea of envelope elimination and restoration, which is being approached in a number of variants. In this idea, the signal is compressed, leaving only the phase information, and the amplitude information is restored by a more or less conventional amplitude modulation process (see ***Figure 2***). Although this approach seems simple and elegant, it suffers from a number of limitations, especially the need for a high efficiency, broadband modulator and the problem of phase shift introduced by the AM modulation process. Much of this can be addressed through DSP techniques. Other methods involve similar, direct phase- and amplitude-modulation of the PA. Again, DSP is necessary to overcome some of the difficulties.

LOW NOISE AMPLIFIERS (LNA)

We have come a long way from the days when a low noise FET cost $300 and provided a 3 dB noise figure at 12 GHz, and we felt lucky to have it. Low noise GaAs, and even InP, FET technologies are mature, epitaxial MESFET technologies have almost completely given way to heterojunction technologies, and such devices are now available in low cost epoxy packages for a few cents each. Device noise figures, in the middle microwave region, are so low that the devices can be viewed as virtually noiseless, in that their noise is negligible relative to other noise sources. Similarly, the large-signal handling of such devices is indeed impressive, although it does come at the cost of DC power. As long as DC power is available, it is relatively easy to realize FET amplifiers with output third-order intercept points (IP3) above 40 dBm, although this generally occurs at some cost to the noise figure. Microwave FET amplifiers still must be optimized for high IP3 or low noise, but cannot be optimized for both. However, low device noise figure means that there is more room to trade off noise figure when the amplifier is optimized for IP3, showing that low noise provides a modest, albeit indirect, distortion benefit. But technical problems, like cockroaches, never disappear; they just find another place to reside. In this case, they have taken up residence in silicon, and now inhabit the land of CMOS and SiGe technology. Device noise figures inevitably fall as technology improves. Now, 0.15 µm CMOS technologies are considered standard tools, and much shorter gate technologies, 0.090 µm and even 0.065 µm, are available. The latter can produce circuits operating well into the millimeter region; indeed, 60 GHz circuits are readily produced in 0.13 µm technology.[4] These technologies are valuable not only for low noise operation at high frequencies; they also provide high



▲ *Fig. 2 Envelope elimination and restoration is a general term for technologies that remove a signal's amplitude information and use it to modulate a high efficiency amplifier.*

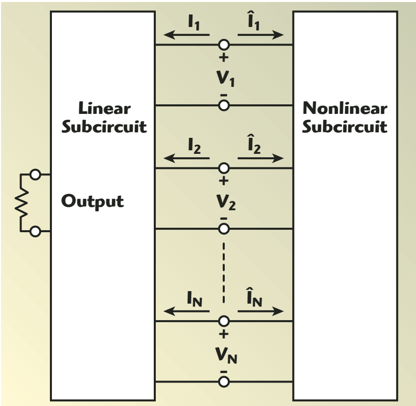
performance at low DC operating power. This is especially important for a wide variety of portable equipment. While reduction in noise figure is automatic as technologies improve, the same is not true of large-signal handling ability. Indeed, if anything, the use of smaller devices and lower operating voltages, necessary for these technologies, results in substantial reduction in large-signal capability. This comes from two characteristics. First, it is possible to show that scaling a particular device to a smaller size inherently decreases its linearity.[5] If this scaling includes reduction in gate length as well as width, the nonlinearity becomes even more pronounced. Second, an amplifier's output power is fundamentally limited by DC input power. As the signal level reaches a point where the amplifier cannot provide more output power, it saturates and the signal is distorted. Thus, even an ideally linear but power-limited amplifier must inevitably generate distortion as its output power approaches its limits. This has profound implications for LNAs in mobile, low power transceivers. Amplifiers in cell phones and computers, for example, must operate at very low DC power, but at the same time, must tolerate strong interfering signals. The communication techniques used in such applications are designed to be tolerant of interference from other users, but they cannot compensate for a signal completely blocking the front-end of the receiver. Thus, large-signal handling is an important requirement for such amplifiers, and, along with all the requirement of low DC power, a difficult one to meet. The DC power limitation is fundamental, so any way around it must involve increasing power, at least temporarily, in some manner. It is interesting to note that the research community seems to be addressing the matter of noise figure through technology improvements, but is not addressing the issue of large-signal handling and linearity in any non-obvious way. It seems, therefore, that some improvements might be possible if more fundamental research were applied to this problem.

OSCILLATOR TECHNOLOGY, DESIGN AND OPTIMIZATION

Oscillators are a mature technology. They have been around for a long time. It would therefore seem that, by now, we should have been able to figure out how they work. But we still have not. Lest the reader dismiss that remark as a provocative overstatement (which it is, after all, but please don't dismiss it quite yet), consider this question: in how many areas of technology do we depend, for design information, on technical concepts that have not changed much in the last 40 years? Kurokawa theory,[7] Barkhausen criterion,[5] describing-function concepts[8] and Leeson's model of phase noise[9] are still the dominant tools for oscillator design. Although it is true that new methods for oscillator and phase noise analysis have been developed,[10–12] these are largely numerical means for computer-aided analysis of such circuits, and, with few exceptions (for instance in Refs. 13 to 17), provide little new, intuitive understanding of these components. Little new information has worked its way into the psyches of designers as general methods for designing and optimizing oscillators. The dominant approach for low noise oscillator design is to create negative resistance, maximize the Q of the tuning circuitry, minimize the noise through device selection, analyze it on the computer (as long as the device model includes low frequency noise sources; most do not) and hope for the best. If some designs work any better than others, it is not because of this kind of design process. One big hang-up is the idea of different types of designs. Four basic design approaches can be described: negative-resistance design, stemming from the ideas first proposed by Kurokawa;[7] the use of Barkhausen's criterion, which is a fundamental idea described in many texts;[8] the use of classical circuit structures such as the Pierce and Colpitts structures; and, finally, the numerical formulations used in circuit simulators, harmonic-balance methods in particular. These have always been viewed as distinctly different design approaches, but, in fact, it is possible to show that they are equivalent. The Colpitts oscillator, for example, can be described as a feedback oscillator with an LC, pi-section feedback circuit.[8,19] Rhea generalized this idea, showing that oscillators could use a wide variety of feedback circuits, many of which

were more appropriate for certain applications or frequency ranges than the classic ones.[20] These were inherently linear designs, but oscillators are strongly nonlinear circuits. These approaches depend on a concept called describing functions, in which the oscillator is modeled in terms of the circuit's effect on the fundamental frequency alone. Although this approach provides some insight into their operation, oscillators, in reality, are nonlinear components and must be treated as such. Describing an oscillator's operation in terms of changes in the fundamental-frequency component and behavior of pseudo-linear poles, as the active part of the circuit goes into oscillation, is a pretty severe oversimplification. Going beyond that kind of description requires consideration of the circuit's nonlinearities. The equivalence of Rhea's generalized feedback circuit (which, recall, is equivalent to the Barkhausen criterion), Kurokawa's negative-resistance approach, and, finally, the modern harmonic-balance approach, are a little more difficult to see. Consider the classical division of a circuit into linear and nonlinear subcircuits for harmonic-balance analysis, as shown in ***Figure 3***. It applies to oscillators as well as driven circuits. In the oscillator case, there are no excitations. (We assume that the DC excitation is inherent in the negative-resistance device and need not to be shown explicitly.) This division is basic to harmonic-balance analysis. Let **Z** be the impedance matrix of the linear subcircuit and **Y** be the admittance matrix of the linearized nonlinear subcircuit. Clearly,

$$\mathbf{V} = \mathbf{ZI} \tag{1}$$



▲ *Fig. 3 The classical division of a circuit into linear and nonlinear subcircuits.*

For oscillation to occur, the voltages at the nonlinear subcircuit must produce the set of harmonic current components that satisfy Equation 1. This is equivalent to saying that the voltage produces a current, from the active element, which in turn produces that same voltage after feedback, a statement, in effect, of the Barkhausen criterion. This is the basis of the feedback description. Thus,

$$-\mathbf{I} = \mathbf{YV} \tag{2}$$

From Equations 1 and 2,

$$-\mathbf{ZYV} = \mathbf{V} \tag{3}$$

Thus, oscillation conditions for the linear oscillator require that the matrix –**ZY** have an eigenvalue equal to 1. Reducing this to Kurokawa's negative-resistance case of a single port and a single frequency (the fundamental, of course), we have

$$-Z_L\, Y_s\, V = V \tag{4}$$

or

$$Z_L = -Z_s \tag{5}$$

which is the well known oscillation condition for negative-resistance oscillators.

This simple derivation also shows why a purely linear oscillator cannot exist: the voltage vectors satisfying Equation 3 are eigenvectors of the system, which are never unique. Thus, a unique oscillatory solution does not exist. Some nonlinearity is necessary to create a unique solution. In the nonlinear case, Equation 3 becomes

$$-\mathbf{Z}\,\mathbf{F_I}(\mathbf{V}) = \mathbf{V} \tag{6}$$

where $\mathbf{F_I}(\mathbf{V})$ is a nonlinear vector function, providing harmonic element currents as a function of harmonic voltages. Although I start to bleed internally while doing this, it is possible to express Equation 6 in this form

$$-\mathbf{Z}\,\mathbf{Y}(\mathbf{V})\,\mathbf{V} = \mathbf{V} \tag{7}$$

generalizing the describing-function approach, which is based on the idea of a fundamental-frequency, psuedo-linear circuit whose admittances depend on voltage magnitude.

NONLINEAR ANALYSIS OF OSCILLATORS

My favorite way to illustrate the problems of nonlinear oscillator

analysis is through an example, the Van der Pol oscillator. The Van der Pol oscillator is beloved of circuit theorists because it can be treated analytically, without resorting to numerical methods. The oscillator is shown in ***Figure 4***. It consists of a nonlinear, negative-resistance device having the I/V characteristic

$$I(V) = -GV + GaV^3 \qquad (8)$$

and an ordinary parallel LC resonator. We assume that this resonator is high Q, so only a single harmonic of voltage can exist; thus,

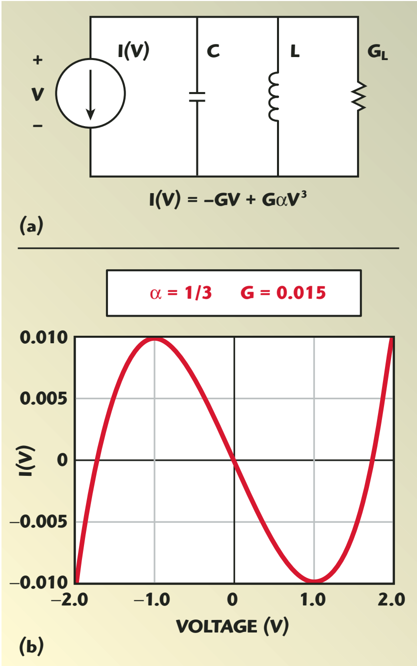
$$V(t) = V_1 \cos(\omega t) \qquad (9)$$

Substituting this into Equation 8 shows that only first- and third-harmonic currents exist, and the latter simply idle in the resonator. Satisfying Kirchoff's current law and solving for V_1 gives the simple result

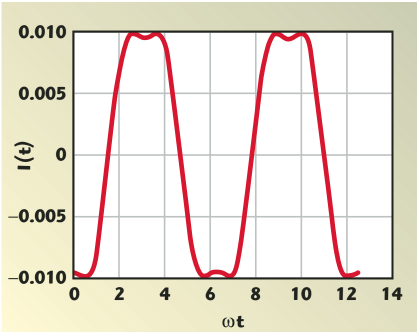
$$V_1 = [4/3\,(G - G_L)/Ga]^{1/2} \qquad (10)$$

Applying some numbers to Equation 10, G = 0.015, G_L = 0.01 and a = 1/3, gives V_1 = 1.1547 V. The device-current waveform is shown in ***Figure 5*** and its fundamental-frequency component is I_1 = –0.01547 A. Note that we have satisfied the oscillation conditions in the negative-resistance sense, as the device admittance (defined as in Kurokawa's theory) is I_1/V_1 = –0.01 = –GL. Note also that the device's small-signal admittance, found by differentiating Equation 8, is –0.015. Thus, the magnitude of the small-signal conductance has decreased, as the voltage magnitude increased, as required by negative-resistance oscillator theory. The figure gives a good, intuitive sense of why this occurs: as V_1 increases, the current waveform flattens, and its fundamental-frequency component no longer increases as rapidly as V_1. Therefore, $|I_1/V_1|$ inevitably decreases, until an equilibrium is reached that satisfies the oscillation conditions. This idea contradicts a commonly held belief about transistor oscillators, namely, that the circuit, unstable in the small-signal sense, "blows up," and is saved from oblivion only by saturation of the active device. In reality, a kind of nonlinear balancing act occurs, with the venerable Kirchoff doing the balancing. The whole process is really quite civilized, and thoroughly non-violent.

The circuit has other stories to tell, which are profoundly important for oscillator analysis. To do so, we put the circuit into harmonic-balance form, create the Jacobian, and discover that, when the oscillation conditions are satisfied, the Jacobian is singular! In practice, this means that oscillator analysis, by harmonic-balance methods, is inherently numerically ill conditioned, and its ill conditioning gets worse as the iterative process approaches a solution. This is one reason why nonlinear analysis of oscillators is so difficult. However, one can also show that when the nonlinear analysis problem is formulated as an optimization problem, instead of the more traditional multi-dimensional Newton approach, the problem is much better conditioned. This may be one reason why methods based



▲ *Fig. 4 The Van der Pol oscillator uses a negative-resistance device that has a particular, cubic, I/V characteristic.*



▲ *Fig. 5 Device-current waveform in the Van der Pol oscillator.*

heavily on optimization, such as the use of an auxiliary generator, seem to be considerably more robust than those based more strongly on Newton's method.

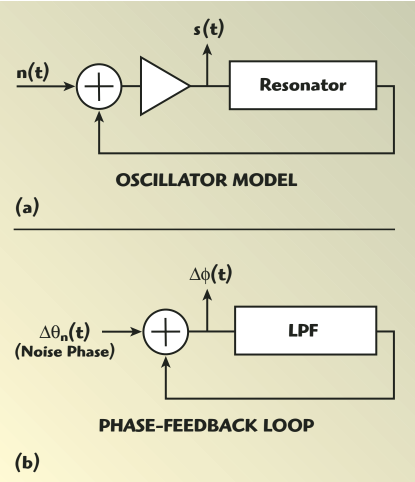
PHASE NOISE ANALYSIS

One of the more contentious research subjects has been the matter of phase noise analysis and optimization. As such, it is interesting to view this situation both historically and technically.

One of the earliest treatments of phase noise in oscillators, and often the only one familiar to designers, is that of Leeson.[9] Leeson formulated the oscillator noise problem as a kind of phase feedback circuit containing an amplifier and resonator, in which noise was treated as an input signal near the frequency of oscillation. The model is shown in ***Figure 6***. Analyzing this model by a baseband equivalent circuit, and assuming the noise spectrum to have a 1/f shape, gives Leeson's well known expression for the SSB carrier-to-noise ratio, $\mathscr{L}(f_m)$,

$$\mathscr{L}\left(f_m\right) = \frac{F}{2P_s}\left(1+\frac{f_c}{f_m}\right)\left[1+\frac{f_0^2}{f_m^2}\frac{1}{4Q_L^2}\right] \tag{11}$$

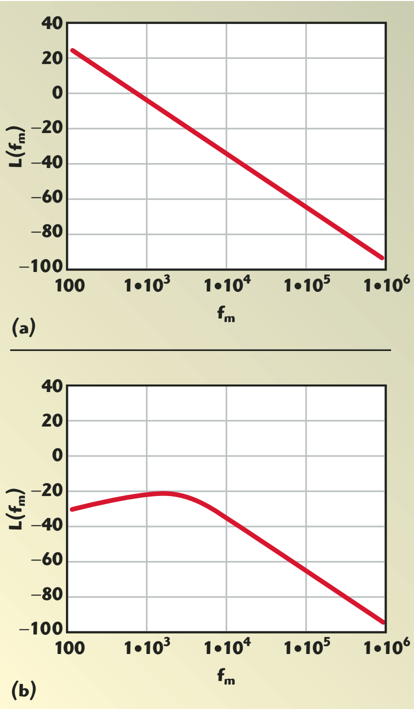
where P_s is the signal power, Q_L is the loaded Q of the resonator, f_m is the offset frequency and f_0 is the frequency of oscillation. F is called the noise figure, but it is actually a measure of the level of upconverted 1/f noise; it is decidedly not the high frequency noise figure of the amplifier.



▲ *Fig. 6 Leeson modeled oscillator noise by a network that included an amplifier and resonator (a); this circuit is reduced to a baseband-equivalent phase-feedback circuit (b).*

This model essentially tells us that, for a particular frequency of oscillation and offset frequency, we should maximize the signal-to-noise ratio and minimize the loaded Q of the resonator, both of which seem intuitively reasonable. The model, however, is not quantitatively very useful, as it does not tell us anything about the upconversion process of 1/f noise from baseband to the oscillation frequency, and the concept of "loaded Q," while clear in the model, is not clear in a real oscillator circuit; the loaded Q of a negative-resistance oscillator is always infinite! Thus, while useful qualitatively, Leeson's model has no real quantitative value.

A more complete phase noise analysis has been a research goal for many years. One of the most interesting early works was that of Rizzoli, et al.,[21] who discovered that ordinary, nonlinear-noise theory, applied to oscillators, simply did not work at low offset frequencies. They did discover, however, that an alternative but equivalent method, based on phase sensitivities, worked well at those small offsets. Thus arose the dichotomy between conversion noise, the standard method and modulation noise, based on phase sensitivities. Many of today's harmonic-balance phase noise analyses still use these



▲ *Fig. 7 Conversion noise calculations of the Van der Pol oscillator phase noise.*

concepts. The problem with conversion noise at small offsets is closely related to the problem of Jacobian singularity. The conversion matrix, used in the conversion-noise analysis, is, in effect, a Jacobian evaluated at the offset frequency. Thus, the smaller the offset, the worse the Jacobian conditioning, and the less stable the solution. This can be illustrated dramatically with the Van der Pol oscillator. ***Figure 7*** shows the results of a conversion-noise analysis of the oscillator (a), which seems quite credible. However, changing a single term of the conversion matrix from 0.005 to 0.005000001 gives the result shown in (b). The original calculation seems right only because the analysis of the Van der Pol oscillator can be performed analytically, and, fortuitously, the matrix entries can be expressed exactly with few decimal places. Note, however, that the graphs are identical beyond 10 kHz. This is typical of conversion-noise analysis. The dual treatment of conversion and modulation noise has always presented a small, but real, dilemma: at what point does one switch from one type of analysis to another? It is not always clear that the intuitive answer to that question is really the correct one. It is better to have one analysis that unifies the two. One such method, which has been implemented in more modern circuit simulators, is that of Ngoya.[22] Experience indicates that this method is quite robust and accurate at all offset frequencies.

OSCILLATOR DESIGN AND OPTIMIZATION

These methods, while important for numerical analysis of oscillators, provide little insight into design techniques for minimizing phase noise. Surprisingly, only a little work based on ideas other than manipulation of Leeson's model has been presented. One exception is the work of Zirath, et al., who showed that millimeter-wave oscillator phase noise, in both SiGe and InGaP HBT technologies, could be minimized through the use of a small set of thoroughly straightforward design methods. One of their VCOs exhibited –120 dBc noise at 100 kHz offset, at an output frequency of 13 GHz.[17,18] One of the clear implications of Leeson's model, as well as other approaches to phase noise analysis,

is the need for a high resonator Q. High resonator Q not only minimizes phase noise, but makes the oscillator's stability (which is, in reality, a kind of phase noise at low offset frequencies) more a function of the resonator's characteristics and less of the device's. The latter, of course, is thermally relatively unstable, so it is beneficial to make the oscillator's performance dependent primarily on a stable, well designed resonator.

Unfortunately, making a good resonator is not easy, especially if small size and complete integration is needed. Most high performance oscillators today use dielectric resonators coupled to microstrip. These must be shielded and located off-chip, so even a monolithic oscillator incurs the cost of a special housing and extra components. Worse, optimizing the dielectric resonator's coupling to the microstrip line usually requires a degree of manual adjustment, the last thing one desires in low cost, high volume production. Thus, the research literature is heavy with attempts to create high quality (or, shall we say, acceptable-quality) resonators on-chip. This need is especially great in silicon RF CMOS and BiCMOS, where virtually every chip needs the high stability, frequency accuracy and low phase noise provided by a phase-locked loop. Inevitably, the on-chip resonator is an LC circuit using a spiral inductor. Because of the inherently lossy substrates and conductors used in CMOS circuits, such inductors do not have high Qs. Much research has been devoted to optimizing those inductors.[23–27] Some of this work has been quite sophisticated analytically,[28] and a wide variety of circuits have been produced.[29–33] Other work has been devoted to finding other ways to make tunable reactive elements[34] or integrating more conventional resonators into fabrication media, obviating the need for resonator tuning.[35]

OSCILLATORS AND AMPLIFIERS AT MILLIMETER WAVELENGTHS

One of the most remarkable developments of the past few years has been the ability to fabricate millimeter-wave (mmW) circuits in silicon CMOS. The sophistication of silicon technology, allowing thin oxides and feature sizes well below 0.1 µm, with good yield, allows practical circuits well above 100 GHz. Although many difficulties remain, such capabilities indicate that commercial mmW applications may exist in the near future. At the same time, modern circuit-analysis and electromagnetic-analysis software is instrumental in addressing the very difficult problems of low cost, practical circuit interfaces and packaging. Automotive applications serve as a prototype for the commercial exploitation of such technologies. The obvious one is the automotive radar band at 77 GHz. GaAs and InP heterojunction technologies have been, and probably always will be, too expensive for making automotive radars that can be installed in all types of vehicles. Silicon will probably be necessary for a broad application of such systems. Similarly, many types of automotive sensors, such as anti-theft devices and backup and

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AMF-4D-00100200-40-27P	0.1–2	40	1.5	4	27	2:1/2.3:1	750
AMF-4D-00100800-40-28P	0.1–8	37	1.5	4	28	2:1	800
AMF-2B-02000800-70-27P	2–8	15	1.5	7	27	2:1	560
AMF-3B-02000800-55-27P	2–8	25	1.5	5.5	27	2:1	660
AMF-4B-02000800-45-27P	2–8	36	1.5	4.5	27	2:1	720
AMF-5B-08001800-80-27P	8–18	20	2	8	27	2:1	1200
AMF-6B-08001800-70-27P	8–18	25	2	7	27	2:1	1300
AMF-7B-08001800-60-27P	8–18	30	2	6	27	2:1	1400
AMF-9B-08001800-70-29P	8–18	30	2.5	7	29	2:1	3000
AMF-1B-01000200-40-25P	1–2	10	1	4	25	2:1	250
AMF-2B-01000200-13-25P	1–2	30	1	1.3	25	2:1	300
AMF-3B-01000200-10-25P	1–2	42	1	1	25	2:1	360
AMF-2B-02000400-30-25P	2–4	22	1	3	25	2:1	330
AMF-3B-02000400-15-25P	2–4	35	1	1.5	25	2:1	400
AMF-4B-02000400-13-25P	2–4	47	1	1.3	25	2:1	440
AMF-3B-04000800-25-25P	4–8	25	1	2.5	25	2:1	450
AMF-4B-04000800-15-25P	4–8	36	1	1.5	25	2:1	490
AMF-5B-04000800-15-25P	4–8	47	1	1.5	25	2:1	540
AMF-6B-12001800-45-25P	12–18	33	1.5	4.5	25	2:1	740
AMF-5B-12001800-60-28P	12–18	18	2	6	28	2:1	1600
AMF-6B-12001800-50-28P	12–18	24	2	5	28	2:1	1700
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blind-spot warning sensors, already exist, albeit only in high end vehicles. Cost reductions likely from silicon mmW realizations may make these more generally available, improving security and safety of many kinds of vehicles. Another important application is millimeter-wave imaging for security purposes. Such systems already exist, but they are often too expensive for small-scale use. One of the most important advantages of mmW technology is the availability of broad bandwidths. This is especially important for one of the more interesting applications, point-to-point and point-to-multipoint high data-rate communications at 60 GHz. The 60 GHz band offers up to 7 GHz of spectrum for such applications. Paradoxically, the high loss caused by oxygen absorption at this frequency often is an advantage. It creates an exponential loss component on top of the ordinary inverse-square loss due to range, which can be used, along with power adjustment, to minimize interference. Such techniques have been of interest to the military, for secure communications, for many years. A recent workshop at the 2006 European Solid-state Circuits Conference in Montreux, Switzerland, showed that, although packaging and interfacing issues remain, silicon IC technologies are largely mature enough for the development of commercial circuits. Papers at the conference described, for example, 20 and 77 GHz automotive sensors[37,38] and a 60 GHz power amplifier[39] with surprisingly good performance. Other conferences and journals have offered similarly encouraging results, including work on the packaging problem.[4,40–50] It appears that millimeter waves may no longer be the perpetual technology of the future.

CONCLUSION

Amplifiers and oscillators, while seemingly mature technologies, are still subjects of great importance and substantial research. Efficiency and linearity in power amplifiers, performance of high frequency LNAs in silicon CMOS, and all aspects of low noise oscillator design and analysis are areas of great interest, both in terms of practical needs and research interest. We should see some exciting results in these areas in the next few years. ■

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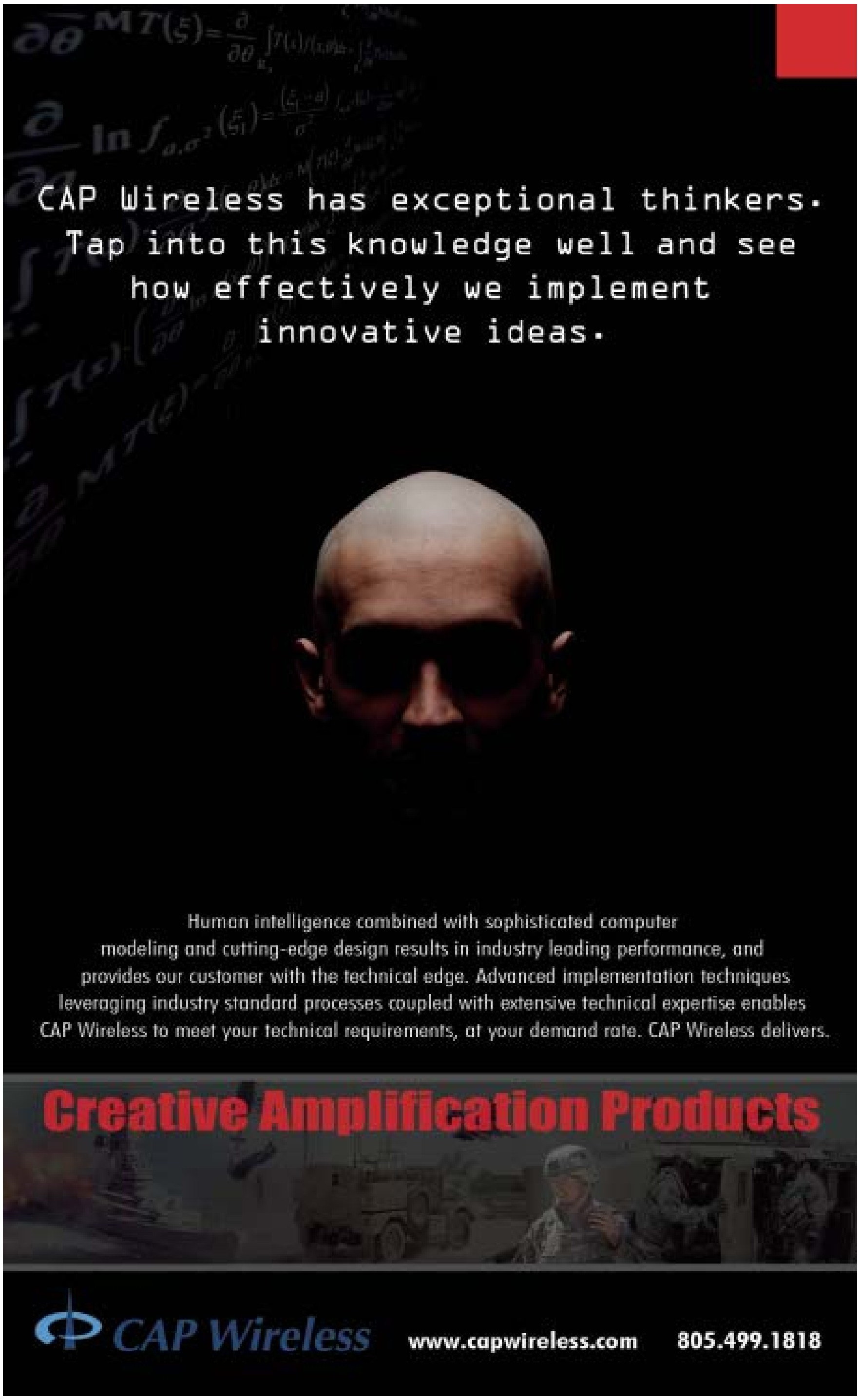

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Broadband Low Noise Amplifiers							
AML016L2802	0.1 – 6.0	28	±1.25	1.3*	+7	2.0:1	190
AML48L3001	4.0 – 8.0	30	±1.0	1.2	+10	1.8:1	150
AML412L3002	4.0 – 12.0	30	±1.5	1.5	+10	1.8:1	150
AML218L0901	2.0 – 18.0	9	±1.0	2.2	+5	2.5:1	60
AML0518L1601-LN	0.5 – 18.0	16	±1.0	2.7	+8	2.2:1	100
AML0126L2202	0.1 – 26.5	22	±2.25	3.5*	+8	2.2:1	170
AML1226L3301	12.0 – 26.5	33	±2.0	2.8	+8	2.5:1	200
Broadband Medium Power Amplifiers							
AML0016P2001	0.01 – 6.0	21	±1.25	3.2*	+23*	2.0:1	480
AML26P3001-2W	2.0 – 6.0	28	±2.5	6	+33	1.8:1	1500
AML28P3002-2W	2.0 – 8.0	30	±2.0	5.5	+33	2.0:1	2000
AML218P3203	2.0 – 18.0	32	±2.5	4	+25	2.0:1	450
AML618P3502-2W	6.0 – 18.0	35	±2.5	4	+33	2.0:1	1850
Narrow Band Low Noise Amplifiers							
AML23L2801	2.8 – 3.1	28	±0.75	0.7	+10	1.8:1	150
AML1414L2401	14.0 – 14.5	24	±0.75	1.5	+10	1.5:1	130
AML1718L2401	17.0 – 18.0	24	±0.75	1.6	+10	1.8:1	150

Low Phase Noise Amplifiers — Phase noise (dBc/Hz) at offset

Part Number	Frequency (GHz)	Gain (dB)	Output Power (dBm)	100Hz	1KHz	10KHz	100KHz
AML811PN0908	8.5 – 11.0	9	17	-154	-159	-167	-170
AML811PN1808	8.5 – 11.0	18	18	-152.5	-157.5	-165.5	-168
AML811PN1508	8.5 – 11.0	15	28	-145.5	-153.5	-158.5	-164.5
AML26PN0904	2.0 – 6.0	9	20	-150	-165	-165	-178
AML26PN1201	2.0 – 6.0	11	15	-155	-160	-160	-175

High Dynamic Range Amplifiers

Part Number	Frequency (MHz)	Gain (dB)	P1dB (dBm)	OIP3 (dBm)	DC
AR01003251X	2 – 32	21	32	52	+28V @ 470mA
AFL30040125	50 – 500	23	28	53	+28V @ 700mA
BP60070024X	20 – 2000	32	30	43	+15V @ 1100mA

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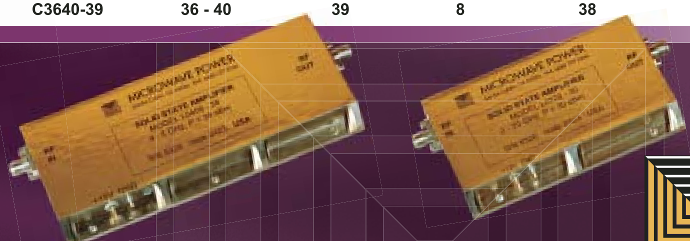
L0104-43	1 - 4	42.5	17.8	41.5	45	14
L0204-44	2 - 4	44	25	42.5	45	14
L0206-40	2 - 6	40	10	38.5	40	8.5
L0208-41	2 - 8	41	12	40	40	17
L0218-32	2 - 18	32	1.4	31	35	5
L0408-43	4 - 8	43	20	41.5	45	17
L0618-43	6 - 18	43	20	41.5	45	22
L0812-46	8 - 12	46	40	45	45	28
Millimeter-Wave Power Amplifiers						
L1826-34	18 - 26	34	2.5	33	35	4
L1840-27	18 - 40	27	0.5	26	30	2
L2240-28	22 - 40	28.5	0.7	27	30	3
L2630-39	26 - 30	39	8.0	38	40	15
L2632-37	26 - 32	37	5.0	36	38	10
L2640-31	26 - 40	31	1.2	30	30	5
L3040-33	30 - 40	33	2.0	32	33	9
L3337-36	33 - 37	36	4.0	35	40	12
L3640-36	36 - 40	36	4.0	35	40	10

High-Power Rack Mount Amplifiers

Model	Frequency (GHz)	Psat (dBm)	Psat (W)	P1dB (dBm)	Pac (kW)	Height (in)
C071077-52	7.1 - 7.7	52.5	170	51.5	1.8	10.25
C090105-50	9 - 10.5	50	100	49	1	8.75
C140145-50	14 - 14.5	50.5	110	49.5	2	10.25
C1416-46	14 - 16	46	40	45	0.35	5.25
C1820-43	18 - 20	43	20	41.5	0.25	5.25
C2326-40	23 - 26	40	10	39	0.25	5.25
C2630-45	26 - 30	45	30	44	0.45	5.25
C3236-40	32 - 36	40	10	39	0.25	5.25
C3640-39	36 - 40	39	8	38	0.24	5.25



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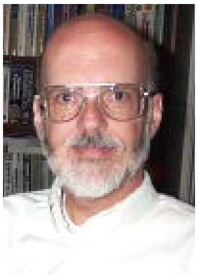

Stephen Maas *received his BSEE and MSEE degrees in electrical engineering from the University of Pennsylvania in 1971 and 1972, respectively, and his PhD degree in electrical engineering from UCLA in 1984. Since then, he has been involved in the research, design and development of low noise and nonlinear microwave circuits and systems at the National Radio Astronomy Observatory (where he designed the receivers for the Very Large Array), Hughes Aircraft Co., TRW, the Aerospace Corp. and the department of electrical engineering at UCLA. Subsequently he worked as an engineering consultant and founded Nonlinear Technologies Inc., a consulting company, in 1993. He recently became chief scientist of Applied Wave Research Inc. He is the author of* Microwave Mixers *(Artech House, 1986 and 1992),* Nonlinear Microwave Circuits *(Artech House, 1988; second edition 2003),* The RF and Microwave Circuit Design Cookbook *(Artech House, 1998) and* Noise in Linear and Nonlinear Circuits *(Artech House, 2005). From 1990 until 1992 he was editor of the* IEEE Transactions on Microwave Theory and Techniques *and from 1990 to 1993 was an Adcom member and Publications Chairman of the IEEE MTT Society. He received the Microwave Prize in 1989 for his work on distortion in diode mixers and the MTT Application Award in 2002. He is a Fellow of the IEEE.*

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AMW/170-2510	14.0 – 17.0	10	0.5	2.5	8
AMM/020-1032	0.5 – 2.0	32	1.0	1.0	8
AMX/0220-4510	2.0 – 20.0	10	2.0	4.5	8

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850 ELSG Office Leads Way in Integrating Radar's Missile Defense

The defense of the United States against potential missile threats is closer to fruition, thanks to the efforts of the 850th Electronic Systems Group's Upgraded Early Warning Radar Program Office, which is charged with incorporating missile defense into existing Air Force early warning radars. "We will have a ballistic missile defense option that allows us to not only identify and track, but also intercept and destroy warheads in flight," said Col. Michael Cox, UEWR program manager.

The office's mission is to sustain the existing large-scale ballistic missile early warning radars for the Air Force while also developing the missile defense capabilities put into these radars for the Missile Defense Agency (MDA). It manages the sustainment and development efforts for six ground-based radars. Four have been or are currently being upgraded—COBRA DANE at Eareckson Air Station, Shemya, AK; Beale AFB, CA; R.A.F. Fylingdales, UK; and Thule Air Base, Greenland. The upgrade effort will eventually include radars located at Cape Cod, MA, and Clear, AK. Incorporating the Missile Defense mission into the Ballistic Missile Early Warning System and PAVE PAWS radars allows offensive responses to shoot down missiles. This will act as the nation's first ballistic missile defense by a ground-based sensor network and feed into the Ballistic Missile Defense System that MDA is also putting in place.

"This new capability allows the war fighter to do something against incoming ballistic missiles," Colonel Cox said. Additionally, the upgrade brings with it capabilities that better equip the war fighter to take on threats. Improved tracking capabilities and a clearer picture will translate into a more thorough battlespace view. "It gives the war fighter more flexibility, and a better view of what the real situational awareness of a threat is," the colonel said.

The radars provide tracking data and estimate launch and impact points of the missile. That data is fed into the Integrated Tactical Warning and Attack Assessment system. Analysis of this information allows for the mobilization of forces—moving equipment and airplanes and providing launched bomber fleets with responses. At the same time, data is passed on to MDA's Ground-based Midcourse communication network. This in turn provides information for the launching and guidance of interceptors against incoming missile threats. And though the entire BMDS is currently in development, Colonel Cox said what lies ahead is equally important. For the system, the future means a continual capability evolution, bringing with it more defensive and offensive options against long-range threats. It also means improvements in radar accuracy and reporting times that will consequently feed into offensive capabilities already in place, he said.

Raytheon Excalibur Successfully Completes Final Testing

Raytheon Co.'s Excalibur precision-guided 155 mm artillery round has passed its final testing hurdle for fielding with the successful completion of a so-called Limited User Test in February at Yuma Proving Ground, AZ. Pending additional system-level certification, Excalibur will be fielded to US Army and Canadian field artillery units. When Excalibur is fielded, it will mark the deployment of the world's first autonomous precision-guided artillery projectile, providing soldiers and Marines with unprecedented fire support accuracy from weapon systems organic to the current Brigade Combat Team Force structure.

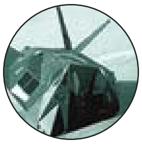
"This is great news from the Excalibur team," said Maj. Gen. David Ralston, commanding general, US Army Fires Center of Excellence. "As the first autonomous guided field artillery projectile, Excalibur provides the users—our field artillery soldiers and Marines—an enhanced capability for responsive, precise and lethal fires in support of the ground commander while simultaneously reducing collateral damage to civilian personnel and facilities."

"Excalibur is out of the lab and in the hands of our soldiers and Marines," said Jim Riley, vice president of the Raytheon Land Combat Product Line. "Excalibur provides the ground commander with a powerful tool to shape the battlefield in real time and dominate the battlespace."

"The successful Limited User Testing was due to hard work on the part of the development team, the Excalibur new equipment training team and soldiers from 1st Battalion, 76th Field Artillery Regiment of the 3rd Infantry Division," Riley said.

"The soldiers operated as truck drivers during their last Iraqi employment. They quickly learned how to use Excalibur with support from the new equipment training team, the unit's soldiers and the user-friendly manner in which Excalibur is integrated into the fire support system. The unit successfully conducted simulated and live Excalibur missions in a tactical environment and is looking forward to using Excalibur in the field," Riley concluded.

With its accuracy and increased effectiveness, Excalibur provides operational flexibility and reduces logistical burden for deployed ground forces. It also significantly reduces collateral damage through increased precision, near-vertical descent and optimized fragmentation pattern. The extended range of the Ia-2 Excalibur (26 miles or 40 km when fired from LW155 and Paladin howitzers), in development now with a planned initial operational capability in fiscal year 2009, will enable positioning of forces and further extend maneuver forces' tactical reach.



Harris Begins Delivery of Large Aperture Multiband Deployable Antennas

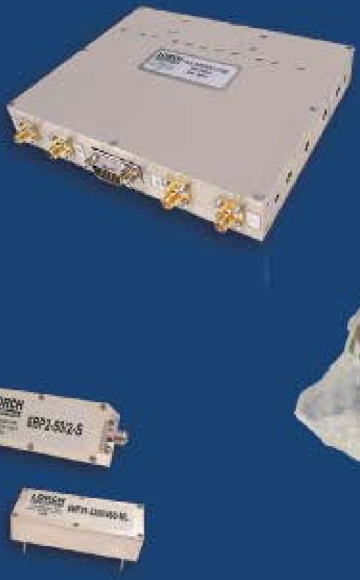
Harris Corp. has delivered the first 12 of 39 Large Aperture Multiband Deployable Antenna (LAMDA) terminals to be used by the US Marine Corps and US Air Force for multiband, mobile satellite communications. The order for 39 LAMDA terminals is part of a $42 M contract awarded to Harris in 2004 by the US Army that also includes 25 Lightweight High Gain X-band Antenna (LHGXA) terminals.

The LAMDA is an enhanced version of the field-proven LHGXA, a rugged, highly mobile tactical antenna deployed and operated by military personnel worldwide. The LAMDA provides field units with user-friendly, large aperture tri-band (C-, X- and Ku-band) antenna that withstands the rigors of harsh operating environments. The terminal supports tri-band operation by using interchangeable antenna feeds that can be rapidly installed by operators in the field. The LAMDA operates with the Defense Satellite Communications System, the Wideband Gapfiller System, NATO, Skynet, XTAR and Intelsat satellite constellations.

"These deliveries represent another key milestone in the LAMDA program, and we expect to continue delivering three systems per month going forward," said Sheldon Fox, vice president and general manager of Department of Defense Programs, Harris Government Communications Systems Division. "The LAMDA demonstrates Harris's ability to expand its proven technology and expertise in satellite communications terminals to a new solution that offers enhanced operational flexibility, greater data rates, improved link reliability and significant satellite-lease cost savings. In addition to its use by US forces, we think LAMDA is ideal for international military applications as well."

Of the 39 LAMDAs currently under contract, 21 will go to the Marines and 18 to the Air Force. Harris has to date delivered nine LAMDAs to the Marines and three to the Air Force. The LAMDA purchases are being made under a larger umbrella contract to the US Army that also covers the purchase of the LHGXA.

The LAMDA incorporates a 4.9 m (16 ft.) diameter reflector mounted on an HMMWV-towable trailer, yet has the equivalent performance characteristics of a 20 ft. reflector due to its shaped, offset-fed design. Rugged, yet lightweight outer panels allow a three-person crew to set up or tear down the antenna in less than 45 minutes. ■



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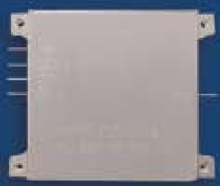
knowledge and experience are ours



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EMSA and ESA Sign Maritime Monitoring Agreement

The European Maritime Safety Agency (EMSA) and the European Space Agency (ESA) have signed an agreement, which strengthens the framework for cooperation between the two organisations in the field of maritime monitoring and surveillance. In particular, EMSA will be supported by ESA on issues relating to the development of space technologies for maritime monitoring and surveillance. In light of its role as a long-term operational European user of satellite technology, EMSA will advise ESA on user requirements for new space systems and infrastructure.

The agreement was signed at the final preparatory stage of EMSA's new satellite-based oil spill monitoring service covering all European waters and adjacent high seas. Under this service, potential oil slicks are detected using satellite radar images and an alert is provided to EU coastal states and EMSA within 30 minutes of the satellite acquiring the image.

Willem de Ruiter, executive director of EMSA, commented, "The agreement with ESA is very valuable for the Agency's new European oil spill monitoring service. ESA's earth observation satellite ENVISAT is an extremely powerful tool that will enable us to provide valuable additional services to EU Member States in the fight to control ship-sourced pollution." For ESA, its director of Earth observation programmes, Volker Liebig, stated, "We see this agreement with EMSA as a major milestone in the operational use of data from Earth observation satellites in Europe."

tbp Acquires Alcatel-Lucent Facility in Belgium

tbp Electronics B.V. has signed a binding Memorandum of Understanding (MoU) with Alcatel-Lucent in Belgium to buy its manufacturing activities at Geel, with the agreement expected to be completed in the second quarter of 2007. A new company—tbp Electronics Belgium—will be formed. The terms of the MoU include the transfer of all customer contracts, the 319 employees and manufacturing assets, with the current management of the manufacturing plant taking an equity stake in the shareholders structure of the new company.

The core business of tbp, which is to provide manufacturing and assembly services for high tech electronic products for the telecom, medical, semiconductor and industrial sector, perfectly fits with the external mission of Geel. Therefore, it is envisaged that the formation of tbp Electronics Belgium together with tbp Electronics B.V. will create one of the major electronics manufacturing providers in the Benelux region with an extensive customer base, complementary know-how and expertise with full flexibility for prototyping and low to medium volume production.

Under the terms of the MoU, Alcatel-Lucent will provide a 'load' commitment for a minimum of three years and shall consider tbp for its new product introduction activities and/or as a pilot production facility and industrialization centre, including for the transfer of technology to larger volume plants when production processes reach maturity.

VTT Packs Suitcase for Herschel/Planck Mission

Commissioned by Alcatel Alenia Space, VTT Technical Research Centre of Finland has designed and constructed the RF Suitcase satellite testing system for ESA's Herschel/Planck mission. The purpose of the RF Suitcase is to demonstrate the RF compatibility between spacecraft and ground stations prior to launch and to test the uplink and downlink functional and performance characteristics. Among others, the values of several tens of configuration parameters for the ground stations are determined, such that each ground station can immediately communicate with the two satellites, once they are released from the launcher.

The RF parts of the RF Suitcase operating in X-band are engineering models that are similar to actual flight hardware. A set of programmable RF attenuators is used to simulate the propagation losses between the spacecraft and ground stations over a distance of about 1.5 million km. These RF parts together with a Telecommand and Telemetry Simulator are integrated into a single transportable cabinet. The cabinet includes a user-friendly control and monitoring subsystem that enables local and remote operation of the RF Suitcase.

The unit was initially supplied for tests in spring 2006 with the final tests at Herschel-frequency planned for summer 2007. Prior to the launch of the real satellites, which is scheduled for mid-2008, the RF Suitcase will be used in various complementary tests to demonstrate that communications between ground stations and the satellites will function.

C-MAC Joins MEAD Consortium

C-MAC MicroTechnology, a world leader in high reliability electronic systems, modules and components for the aerospace, automotive, industrial, medical and communications markets, has been selected as a partner in the MEMS Application for Defence (MEAD) consortium, led by QinetiQ. The consortium will develop microelectromechanical systems (MEMS) technology for the defence industry in a project backed by the UK MoD, with £3.2 M of funding over three years.

The MEAD consortium brings together world-class organisations spanning systems integration and MEMS device supply, including key groups from the world of academia and research. Initially, it will roadmap the technology, explore exploitation routes and investigate novel MEMS approaches for use in key defence application areas.

C-MAC's role will be to use its MEMS packaging expertise to provide the consortium with high reliability hermetic enclosures for the delicate MEMS devices, protecting them from environmental contamination and ensuring their integrity in the harsh environments in which they will operate. The company was chosen as it has demonstrated the ability to deliver robust, precision electronic modules, which are reliable under the most severe conditions experienced by electronic devices in defence applications.

Indro Mukerjee, CEO of C-MAC MicroTechnology, commented, "C-MAC has worked in the defence sector and with QinetiQ for several years and we have a thorough understanding of their stringent technical and operational requirements. MEMS technology is experiencing an exciting and progressive stage of evolution, and being invited to join the MEAD consortium is a reflection of the world class expertise and knowledge that C-MAC engineers can deliver in this area."

Saab Wins Estonian Air Defence Contract

The Estonian government has signed the contract for the new Estonian Air Defence System—the Very Short Range Air Defence Missile System (VSHORADMS). Following fierce competition between leading European and US defence companies the contract, valued at around €60 M, was awarded to MBDA and Saab. The VSHORADMS is based on MISTRAL missiles from MBDA, Giraffe AMB radars, command and control centers, and a communication system, including NATO links from Saab Microwave Systems.

The 3D Multirole Giraffe AMB search and surveillance radar, which is a vital part of the system, belongs to the latest generation of Saab's ground-based surveillance radars. When delivered the VSHORADMS system will be fully NATO compatible by using NATO data links such as Link 11B and LLAPI, integrated by Saab Microwave Systems.

Mikael Johannison, head of sales for Baltic and Central Europe at Saab Microwave Systems, said, "Estonia's selection of Saab for this contract is an important milestone for us in providing tailor-made ground-based air defence systems." ■

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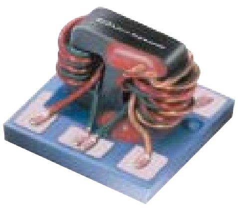

Model	Freq. (MHz)	Z	Price $ea. (Qty. 25)
SBTC-2-10+	5-1000	50 Ω	2.49
SBTC-2-20+	200-2000	50 Ω	3.49
SBTC-2-25+	1000-2500	50 Ω	3.49
SBTC-2-10-75+	10-1000	75 Ω	3.49
SBTC-2-15-75+	500-1500	75 Ω	3.49
SBTC-2-10-5075+	50-1000	50/75 Ω	3.49
SBTC-2-10-7550+	5-1000	50/75 Ω	3.49

U.S. Patent No. 6,963,255

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GaAs Will Remain at Forefront of Cellular Handsets

Strategy Analytics analysts, speaking at the plenary sessions of both the IEEE CSIC Symposium and the Power Amplifier Symposium, reaffirmed that GaAs technologies will continue to dominate the radio front-end in cellular handsets, despite competition from silicon technologies. The move toward 3G and beyond, coupled with the need to maintain backwards compatibility, has led to multi-mode and multi-band architectures, while increasing requirements for linear performance and efficiency in the power amplifier (PA). According to Asif Anwar, director, GaAs and Compound Semiconductor Technologies for Strategy Analytics, "GaAs is often portrayed as an expensive, exotic technology, but the reality is that GaAs continues to meet the challenges of cost, packaging, time-to-market and integration for the cellular handset market. LTE (long term evolution) and beyond will lead to even higher frequencies and data rates and the PA will continue to be the critical component in mobile phones through 2012." Stephen Entwistle, vice president of the Strategy Analytics Strategic Technology Practices, adds, "W-EDGE has emerged as the de facto standard for new handsets operating across multiple regions by supporting W-CDMA, EDGE and legacy GSM and GORS modes. Moving forward, Strategy Analytics expects to see the emphasis on multi-mode operation to remain vital for handset OEMs." A précis of the presentation, "Challenges and Opportunities for Compound Semiconductors in the Mobile Handset Roadmap," is available at www.strategyanalytics.net.

Wireless Sensors Offer Efficiencies and Savings for Process Monitoring

Those who remember the night of December 2, 1984, when water accidentally entered a methylisocyanate storage tank at a Union Carbide factory in Bhopal, India, will understand the importance of monitoring industrial processes. Gauges measuring the temperature and pressure were known to be unreliable, so staff ignored early signs of trouble and a cloud of toxic gas rolled across the crowded working-class district. In what has been called the world's worst industrial accident, at least 3000 died and hundreds of thousands were injured. The factory was subsequently closed down. Clearly, reliable industrial monitoring systems are critical and according to ABI Research analyst Sam Lucero, "Wireless monitoring systems increase the number of monitoring points that you can deploy. You can get more information about your processes, using fewer employees and without having to check instrument readings manually." A new study from ABI Research analyzes the global market for wireless, networked industrial monitoring. Two of the leading wire industrial monitoring system vendors—Emerson and Honeywell—have introduced wireless monitoring technology and more wireless product introductions are expected in the next few years from other vendors as well. Furthermore, a wireless extension to the ubiquitous HART protocol, which is the basis of most industrial monitoring networks, is expected this summer, along with an ISA SP-100.11a standard expected in 2008 and "industrial-grade" ZigBee trying to gain traction. Although this is an intrinsically cautious industry, notes Lucero, "We do expect a fairly strong growth rate, owing to the financial benefits and ease of deployment wireless technology provides. We saw about 100,000 802.15.4 chipsets going into the industrial sector in 2006; that will rise to almost five million in 2012. Some of that growth will be based on replacement of wire process monitoring nodes, some will be from an increase in total process monitoring nodes enabled by the use of wireless technology and some will be growth due to the use of wireless technology in condition monitoring applications." ABI Research's Wireless Sensor Networking (WSN) in Industrial Automation analyzes the market opportunities for industrial deployments, detailing where it will find traction (and where it will not); the implications of the key standard efforts including Wireless HART, Sp-100.11a and industrial ZigBee; the implications WSN adoption will have for the market; and the key players involved in making WSN a reality in industrial automation. It forms part of two ABI Research Services, M2M and Short-Range Wireless.

Mobile Operators to Invest $18 B in UMTS LTE Networks by 2014

Long Term Evolution (LTE) of 3G technologies is about to benefit from Rel-8 of the 3GPP standard, planned for the third quarter of 2007. This will be the trigger for development of components and systems to provide 100 Mbps download speeds to mobile devices. According to a new study from ABI Research, network operators will invest a total of almost $18 B in LTE capital infrastructure over the period to 2014. This will yield a significant payoff, both in reduction of operating expenses and in the creation of new revenue from IP-based services. "LTE faces competition from other broadband wireless technologies and it will need to demonstrate clear technical and economic advantages to convince network operators," says ABI Research analyst Ian Cox. "WiMAX has a two-year lead over LTE but suffers from not being backwards-compatible with current 3G technologies. LTE will not only be backwards-compatible with UMTS but is likely to be used to upgrade CDMA networks as well. But the industry is also working on HSPA+, which could offer the same performance in a 5 MHz bandwidth. Without additional spectrum, operators face a difficult choice." Cox further comments that, "The industry is also making progress in avoiding intellectual property rights issues in the new standard. Next generation mobile networks (NGMN) have been set up by leading operators to ensure a level playing field." For users, says Cox, LTE will enable broadband services, including VoIP, to be offered over SIP-enabled network. Each service will be IP-based, offering high data rates and low latency, with on-line gaming becoming a reality, along with mobile network data speeds comparable to those of fixed networks. For vendors, LTE will allow development of a new market to replace 3G revenues. For operators, an all-IP network with simpler, flat architecture will reduce operating costs and boost revenues.

Technology Does Not Matter!

These are the words that can label you as a non-believer and a heretic. For the telecom industry, thoughts like this must be exterminated before they spread like a virus. Yet, recently an example of how little technology matters surfaced. Deutsche Telekom (DT) killed its Fixed-Mobile Convergence (FMC) service. The FMC service, named T-One, was offered by the wireline division of Deutsche Telekom in Germany. Since its introduction in August 2006, the WiFi/GSM service attracted only 10,000 subscribers. The reasons for the failure range from high prices, poor marketing, minimal features and the lack of alternative handset models. Competition from the cheaper T-Mobile Fixed-Mobile Substitution (FMS) service is also blamed. The @home service bills cellular calls made from home as fixed-line calls. In-Stat Research has consistently found strong consumer interest for both FMC and FMS services. Over 57 percent of broadband households in North America have a strong interest in Home/Zone FMS services. Nearly 40 percent favor making VoWLAN calls from a mobile handset. Yet, consumers indicate their interest in FMC/FMS services is driven by greater convenience and value, not technology. Deutsche Telekom lost sight of this fact when they introduced its FMC service. Other FMC service offerings sporting premium prices or nifty new roaming technology will likely follow in DT's path. Ultimately, service providers will understand that the value of convergence is simplicity. The way to increase ARPU is by giving customers what they want, regardless of technology. ■

INDUSTRY NEWS

■ **Laird Technologies**, a designer and manufacturer of antenna solutions, electromagnetic interference (EMI) shielding products, telematics, signal integrity products and thermal management solutions, announced the acquisition of **AeroComm** for $38 M.

■ **Spectrum Control Inc.**, a designer and manufacturer of electronic control products and systems, announced that **Spectrum Microwave Inc.**, its wholly owned subsidiary, has acquired substantially all of the assets and assumed certain liabilities of **EMF Systems Inc.** (EMF). EMF, based in State College, PA, designs and manufactures custom oscillator-based products, including phase-locked oscillators and synthesizers. The total purchase price of the acquisition was approximately $2.3 M.

■ **Vectron International**, a leader in the design, manufacture and marketing of frequency control, sensor and hybrid product solutions, announced it has completed the acquisition of **BiODE Inc.**, a designer and manufacturer of fluid viscosity sensors and viscometer readers. The BiODE organization will be integrated into Vectron's Sensors and Advanced Packaging (SAP) business unit. The deal represents the company's continued commitment to driving change and innovation in the $50 B global sensor market through the delivery of ground-breaking acoustic wave sensor technology. Customers will now have access to first-of-its-kind fluid viscosity monitoring technology that delivers time and cost savings as well as increased scalability.

■ **Fluke Corp.**, a leader in portable, professional electronic test tools, announced the acquisition of **DH Instruments Inc.** (DHI). DHI is a manufacturer of high performance pressure and gas flow standards, including calibration process software. DHI also offers A2LA accredited pressure and gas flow calibration services, as well as metrology training courses at its facility in Phoenix, AZ. Under the agreement, DHI will become part of the Fluke Precision Measurement division, joining the Fluke calibration product and service teams.

■ **Wurth Elektronik eiSos Group** announced the acquisition of **Midcom Inc.** The previous owner, the Holien Group, sold the transformer division for strategic reasons. Midcom Inc. is based in Watertown, SD, with the majority of the staff employed in the production facilities in Longgang near Shenzhen and in Fuling near Chongqing, China.

■ **Silicon Laboratories Inc.**, a leader in high performance, analog-intensive, mixed-signal integrated circuits (IC), announced a definitive agreement with **NXP**, formerly Philips Semiconductor. NXP will purchase the Aero transceiver, AeroFONE™ single-chip phone and power amplifier product lines, for $285 M in cash, with additional earn-out potential of up to an aggregate of $65 M over the next three years.

■ **Harris Corp.** and **Stratex Networks Inc.** announced the completion of the transaction that has created a new company—**Harris Stratex Networks Inc.** The new company brings together the former Harris Microwave Communications Division and Stratex Networks Inc. The new company, with calendar year 2006 revenue of about $650 M, is the largest independent provider of wireless transmission network solutions, with customers in over 150 countries.

■ **Bliley Technologies Inc.**, an international provider of crystal-based frequency control solutions, and **Allan Space-Time Solutions LLC**, led by renowned atomic clock physicist, David W. Allan, have teamed up to form a new, co-owned company, **EQUATE Space-Time Technologies LLC**. EQUATE Space-Time Technologies' immediate plans include development of a test system to prove the company's technology concepts.

■ **Power Module Technology Inc.** (PMT), formerly IMT RF Products, announced the teaming of solid-state RF power industry veterans, Terry Simons, Bobby McDonald, Dave Gill and Sam Klein. PMT's focus is to provide customers with RF power pallets and modules that are high power, wideband and highly reliable. These cost-effective, 50 ohm building blocks serve a multitude of applications for the broadcast, industrial, scientific and military markets. The company's established high volume manufacturing capability, combined with quick turn-around development capability, allows PMT to offer customer specific products as well as a wide range of standard RF power products. The company is located in Carson City, NV. For more information, visit www.PMTRF.com.

■ **Andrew Corp.** has significantly expanded its strategic relationship with **PCT International Inc.** and its holding company, **Andes Industries Inc.**, through an agreement that will combine the companies' broadband cable assets and create the first global entity that provides complete last-mile cable connectivity solutions to the broadband industry. Under terms of the agreement, Andrew will receive approximately $16 M in cash and short-term notes, and will convert an existing note from Andes into a 30 percent equity stake in Andes, a Gilbert, Arizona-based developer, manufacturer and distributor of products for broadband communications networks.

■ **Nurad Technologies**, a division of Cobham Defense Electronic Systems, announced the recent acquisition of a new 10 foot diameter by 20 foot length autoclave. This autoclave will provide Nurad with the capability to manufacture large RF composite structures (up to 8' × 18'), as well as providing additional manufacturing capacity for smaller products. Nurad designs and produces state-of-the-art composite structures for use in RF and millimeter-wave antenna systems. These structures are built with the latest materials and are designed using a proven, Cobham developed electromagnetic simulation tool that yields first pass success on complex shapes. This new addition to the Baltimore, MD facility enables Nurad to offer the high quality, high performing composite structures demanded by the largest antenna systems.

Cable Construction

Type	Frequency (GHz)	Inner Conductor	Dielectric	Jacket
SF Series	DC-18	Solid Silver-Plated Copper Clad Steel	Solid PTFE	Blue FEP
SFR Series	DC-8	Stranded Silver-Plated	PTFE	Gray PVC

Connectors

Gold Plated Brass Center Contact
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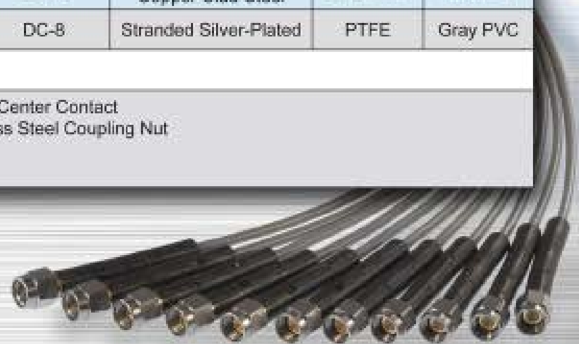
Captive Contacts
PTFE Dielectric



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2. ***Heat Shrink Tube With Built-In Adhesive for added durability.***
3. ***Rugged Construction.***
4. ***Excellent Shielding Effectiveness.***
5. ***Wide Frequency Range.***
6. ***RoHS Compliant.***
7. ***-55°C to +105° Storage & Operating Temperature.***

Model #	Frequency (GHz)	Length** (ft.)	Connector (Male)	Price * Qty. 1-9
SF2-SMSM	DC-18	2	SMA - SMA	$44.95
SF3-SMSM	DC-18	3	SMA - SMA	$52.95
SF2-SMNM	DC-18	2	SMA - Type N	$72.95
SF3-SMNM	DC-18	3	SMA - Type N	$77.95
SFR2-SMSM	DC-8	2	SMA - SMA	$26.95
SFR3-SMSM	DC-8	3	SMA - SMA	$29.95

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■ **RF Micro Devices Inc.** (RFMD) announced the official opening of its new customer support center in Shanghai, China. The new facility underscores RFMD's growing presence in Greater China and the company's commitment to expansion in the world's largest market for cellular handsets. The new center will expand RFMD's capacity to support wireless customers throughout the Far East by expanding and complementing RFMD's operations in Beijing and Shenzhen, China, and Taipei, Taiwan.

■ **Provigent**, a provider of system-on-a-chip (SoC) solutions for the broadband wireless transmission market, has moved its offices from Los Altos to Santa Clara, CA. The new office details are: Provigent Inc., 3333 Bowers Avenue, Santa Clara, CA 95054 (408) 701-2250, fax: (408) 715-0188.

■ **RF Monolithics Inc.** (RFMI) announced the acceleration of the restructuring plan for its components business. This restructuring includes completing the process of outsourcing all Dallas, TX manufacturing and becoming fabless. The company expects to increase the profitability of the components business by leveraging existing lower-cost contract manufacturing relationships. This action will enable the company to increase its focus on the wireless solutions business.

■ **American Technical Ceramics** (ATC), a manufacturer of high performance electronic components, including capacitors and thin film circuits for a broad range of commercial and military applications, announced the official commencement of an outsourced passive component finishing and assembly operation in Costa Rica. ATC will be working with **CAMtronics s.a.**, an electronics contract manufacturing firm located in the Zeta Free Zone Industrial Park in Cartago, Costa Rica.

■ **Auriga Measurement Systems LLC** announced that it has entered into a multi-year research project with **Delft University of Technology**, The Netherlands, on development of RF characterization and modeling tools. Auriga hopes to have the university's initial efforts on display at the MTT show in Hawaii this year.

■ **QUALCOMM Inc.** announced the expansion of its product roadmap to include HSPA+. The next generation of WCDMA systems, HSPA+ delivers broadband mobility at unparalleled data speeds and a superior user experience for applications such as Internet browsing, realtime location services, multimedia sharing and other services that can become a fundamental part of everyday life with the freedom that mobility can offer. QUALCOMM will sample the Mobile Data Modem™ (MDM™) MDM8200™ solution, a chipset supporting HSPA+, by the end of 2007. The MDM8200 solution will support deployments in existing frequency bands, as well as in the 2.5 GHz IMT-2000 extension band.

■ **White Mountain Labs**, an innovative leader in test and characterization of advanced technologies, announced that its new lab facility, The Center for ESD, has

been certified as a suitable lab by the US Defense Supply Center, Columbus (DSCC).

CONTRACTS

■ **Agilent Technologies Inc.** announced that it has been awarded a $12.6 M contract by **Raytheon Co.**, Tucson, AZ. Under the contract, Agilent will deliver an advanced, next-generation automated manufacturing test platform. Raytheon expects this new platform to provide benefits in cycle time, test equipment utilization and labor content.

■ **Merrimac Industries Inc.** announced that it has received an order for $430,000 to supply several Multi-Mix® Microtechnology products for a next generation military communications satellite program. The satellite communications system is designed to significantly improve communications for mobile US forces. Merrimac was selected based on the company's ability to provide dividing and combining devices that are able to handle high RF power, provide low insertion loss, and are contained within a caseless fusion bonded assembly. The program significantly improves communications for warfighters while maintaining backward compatibility to the existing communications systems for the US Department of Defense.

■ **Elcom Technologies Inc.** announced the receipt of an order valued at $428K from **Rockwell Collins** in support of the FAB-T program. The order was for a quantity of Elcom's ruggedized type synthesizer. This is a follow-on order, which Elcom previously received last year, which was valued at approximately $819K.

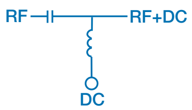
■ **W.L. Gore & Associates** has been awarded the contract to provide GORE™ Umbilical Assemblies for the A-10 Precision Engagement (PE) Kit by **Lockheed Martin**. This is the second contract awarded to Gore for the A-10 program following the initial award of PE kits to the A-10 Prime Team in March 2005.

FINANCIAL NEWS

■ **Fairchild Semiconductor** announced the successful completion of the previously-announced tender offer by one of its wholly owned subsidiaries to acquire up to 100 percent of the outstanding shares of **System General Corp.** for NT$93 per share.

■ **Tower Semiconductor Ltd.** reports sales of $187.4 M for the year end 2006, compared to $94 M (excluding $8 M income in 2005 from a technology-related agreement) for the same period in 2005. Net loss for the year was $87 M ($1.05/per share), compared to a net loss of $203 M ($3.06/per share) for year-end of last year.

■ **Silicon Laboratories Inc.** reports sales of $111 M for the fourth quarter ended December 30, 2006, compared to $110 M for the same period in 2005. Net income for the quarter was $5.2 M ($0.09/per diluted share), compared to $15.3 M ($0.27/per diluted share) for the fourth quarter of last year.



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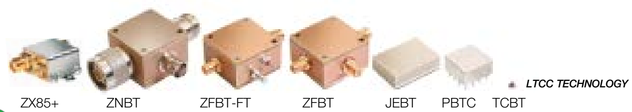
TYPICAL SPECIFICATIONS

Model	Freq (MHz)	Insertion Loss (dB)	Isolation (dB)	VSWR (:1)	Price $ea. Qty.10
TCBT-2R5G	20-2500	0.35	44	1.10	6.95*
TCBT-6G	50-6000	0.7	28	1.20	9.95
TCBT: LTCC, Actual Size .15"x.15", U.S. Patent 7,012,486.					**Qty.1-9**
JEBT-4R2G	10-4200	0.6	40	1.10	39.95
JEBT-4R2GW	0.1-4200	0.6	40	1.10	59.95
PBTC-1G	10-1000	0.3	33	1.10	25.95
PBTC-3G	10-3000	0.3	30	1.13	35.95
PBTC-1GW	0.1-1000	0.3	33	1.10	35.95
PBTC-3GW	0.1-3000	0.3	30	1.13	46.95
ZFBT-4R2G	10-4200	0.6	40	1.13	59.95
ZFBT-6G	10-6000	0.6	40	1.13	79.95
ZFBT-4R2GW	0.1-4200	0.6	40	1.13	79.95
ZFBT-6GW	0.1-6000	0.6	40	1.13	89.95
ZFBT-4R2G-FT	10-4200	0.6	N/A	1.13	59.95
ZFBT-6G-FT	10-6000	0.6	N/A	1.13	79.95
ZFBT-4R2GW-FT	0.1-4200	0.6	N/A	1.13	79.95
ZFBT-6GW-FT	0.1-6000	0.6	N/A	1.13	89.95
ZNBT-60-1W	2.5-6000	0.6	45	1.10	82.95
ZX85-12G+	0.2-12000	0.6	N/A	1.20	99.95

ZX85: U.S. Patent 6,790,049.

Note: Isolation dB applies to DC to (RF) and DC to (RF+DC) ports.



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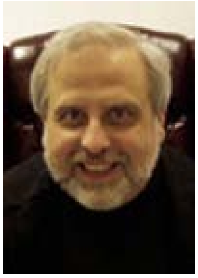
Around the Circuit

■ **ANADIGICS Inc.** reports sales of $49.1 M for the fourth quarter of 2006 ended December 31, 2006, compared to $33.3 M for the same period in 2005. Net loss for the quarter was $0.1 M ($0.00/per share), compared to a net loss of $3.9 M ($0.11/per share) for the fourth quarter of last year.

■ **Ansoft Corp.** reports sales of $22.7 M for the third quarter of fiscal 2007 ended January 31, 2007, compared to $19.7 M for the same period in 2006. Net income for the quarter was $6.3 M ($0.24/per diluted share), compared to a net income of $4.3 M ($0.16/per diluted share) for the third quarter of last year.

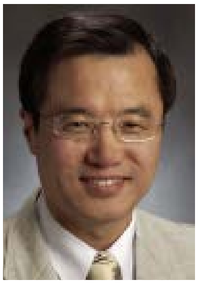
■ **RF Industries Ltd.** reports sales of $4.1 M for the fourth quarter ended October 31, 2006, compared to $3.4 M for the same period in 2005. Net income for the quarter was $473,000 ($0.13/per diluted share), compared to a net loss of $119,000 ($0.04/per diluted share) for the fourth quarter of last year.

PERSONNEL



▲ Jerry Brown

■ **Jerry Brown** has been named president of LBA Technology Inc., an international supplier of communications products and infrastructure. Since August of 2005, he has held the position of vice president of sales for the LBA Group, including both LBA Technology Inc. and Lawrence Behr Associates Inc.



▲ Seri Lee

■ Nextreme Thermal Solutions, a manufacturer of advanced thin film thermoelectric components designed and produced to address the thermal management needs of the electronics, photonics, bio-tech and defense/aerospace industries, has recently appointed **Seri Lee** as chief technology officer. Prior to joining Nextreme, Lee served as senior thermal scientist for the Silicon and Platform Solutions Group at Intel Corp., where he was responsible for executing corporate thermal directions for consumer products and technology development requirements.

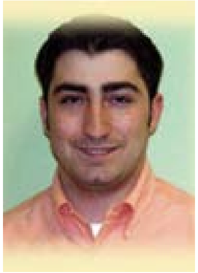
▲ Daniel Ziroli

■ International Manufacturing Services Inc. (IMS) announced the appointment of **Daniel Ziroli** to director of sales and marketing. Ziroli brings more than 30 years of electronics industry experience to IMS, and has served in a number of senior sales and management positions for companies including SRC Devices, Crydom Corp., Douglas Randall and Elmwood Sensors.

■ Cobham Defense Electronic Systems announced the addition of **Dennis "Denny" Mitchell** as director, sales and marketing Nurad Technologies. Mitchell brings over 30 years of experi-

ence in the field of microwave communications and antenna experience to Nurad. He was formerly a design engineer for Raytheon's RADAR Receiver lab in Wayland, MA. Mitchell also founded Microwave Research and Manufacturing, a subsystems house in Hopkinton, MA, and was a vice president of millimeter-wave products for the OMRON Corp.

■ Q Microwave Inc. announced the appointment of **Dan Czagany** as sales manager of the company. With more than 25 years of marketing and sales experience within the RF and microwave industry, Czagany brings a wealth of knowledge to the company's growing business opportunities. His experience includes sales of a variety of microwave components and subsystems for military, industrial and commercial applications. His past positions were with companies including REMEC Defense and Space Inc., KW Microwave Inc., Integrated Microwave Corp. (IMC) and Andersen Laboratories.


▲ Gabe Romero

■ Renaissance Electronics announced the appointment of **Gabe Romero** to the sales staff. Romero is a 2005 graduate of MIT and will be a member of the RF subsystems product group. His main focus will be supporting existing base station product customers in North America.

REP APPOINTMENTS

■ Electronic component distributor **Digi-Key Corp.** and **FlexiPanel** announced the signing of a global distribution agreement. FlexiPanel develops wireless ZigBee and Bluetooth solutions, and provides a seamless wireless integration solution for developers of not only microchip MCUs but also developers who are not generally familiar with RF. FlexiPanel's products provide a simple path to add ZigBee or Bluetooth to an existing or new product and reduce the design/software knowledge requirement by including the ZigBee and Bluetooth software stacks on the MCUs.

■ **TRAK Microwave Corp.** announced the appointment of **Broadband Technical Sales** as the company's exclusive sales representative in northern California. Broadband will represent TRAK Microwave Corp.'s microwave products. Broadband can be reached at: Broadband Technical Sales, 1745 Saratoga Avenue, Suite 206, San Jose, CA 95128 (408) 813-5000, e-mail: john@broadbandtech.com or visit www.broadbandtech.com.

■ **precisionWave Corp.** announced the selection of **Sellex Corp.** as its exclusive sales representative in the Republic of Korea. Sellex is a dynamic, full service, high technology manufacturer's representative and export management firm specializing in the Republic of Korea's (South Korea's) high technology industries with offices located in Seoul, Korea and Las Vegas, NV. Sellex will promote, sell and support precisionWave's line of low cost, high performance RF test instruments.

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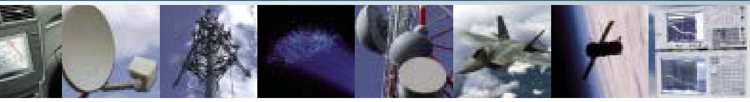

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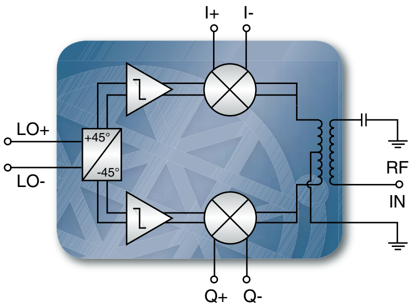

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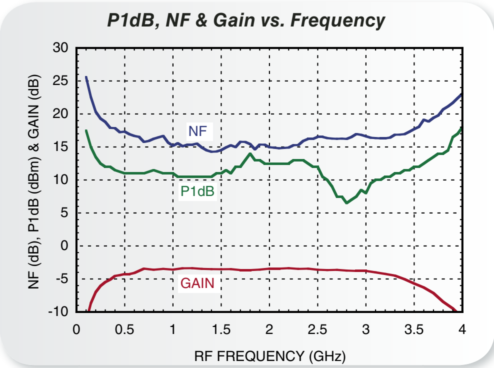

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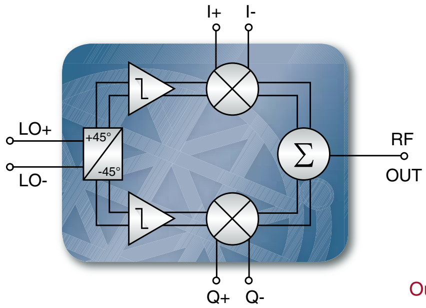

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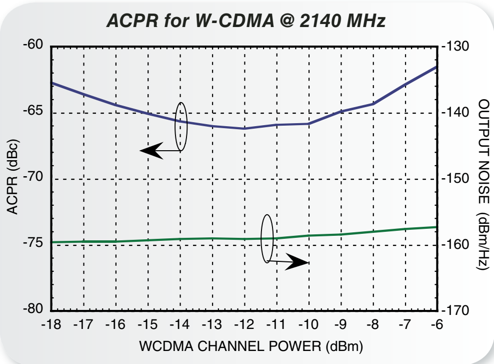

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AN ENHANCED DOHERTY AMPLIFIER DESIGN BASED ON THE DERIVATIVE SUPERPOSITION METHOD

An enhanced 20 W Doherty amplifier with highly optimized linearity using the derivative superposition method (DSM) is proposed. DSM is a linearization technique based on the device's transconductance characteristics. The gain compression of the main amplifier, biased in class AB, can be compensated by combining it with the gain expansion of the peaking amplifier, biased in class C. The adjacent channel leakage power ratio (ACLR) performance of the Doherty amplifier is optimized by adjusting the offset lines, shunt capacitors and gate biases. The shunt capacitors are an important parameter to achieve optimum linearization performance in the Doherty amplifier. The results, measured on an optimized Doherty amplifier for a single-carrier WCDMA signal, achieved –45 dBc ACLR at a ±5 MHz offset frequency. This is an ACLR improvement of 16.7 dB in comparison to the Doherty amplifier before optimization. The digitally pre-distorted optimized Doherty amplifier achieved an ACPR of –52.5 dBc at a ±2.5 MHz offset frequency.

High linearity and high efficiency are important design issues in a high power amplifier for base station applications in modern wireless communications. High efficiency power amplifiers, combined with high linearity, have been very desirable. The Doherty amplifier is a technique for improving the efficiency at high output power back-off.[1] Unfortunately, the Doherty amplifier has a poor intermodulation distortion (IMD) performance when the main and peaking amplifier's signals are recombined at the output, using load modulation. This is because the peaking amplifier biasing mode is in class C, which generates high order IMD products.

In order to improve the linearity of a Doherty amplifier, a number of practical system-level techniques have been proposed: analog pre-distortion (APD), digital pre-distortion (DPD) and feed-forward linearization.[2–4] Doherty amplification combined with analog pre-distortion has a simple operation, but its linear performance is limited. Digital pre-distortion and feed-forward linearization, when used in conjunction with a Doherty amplifier, provide good linearity. However, they have the disadvantage of bulky size and complex circuitry. The inherent linearity deterioration of a Doherty amplifier sets a threshold for achievable performance.

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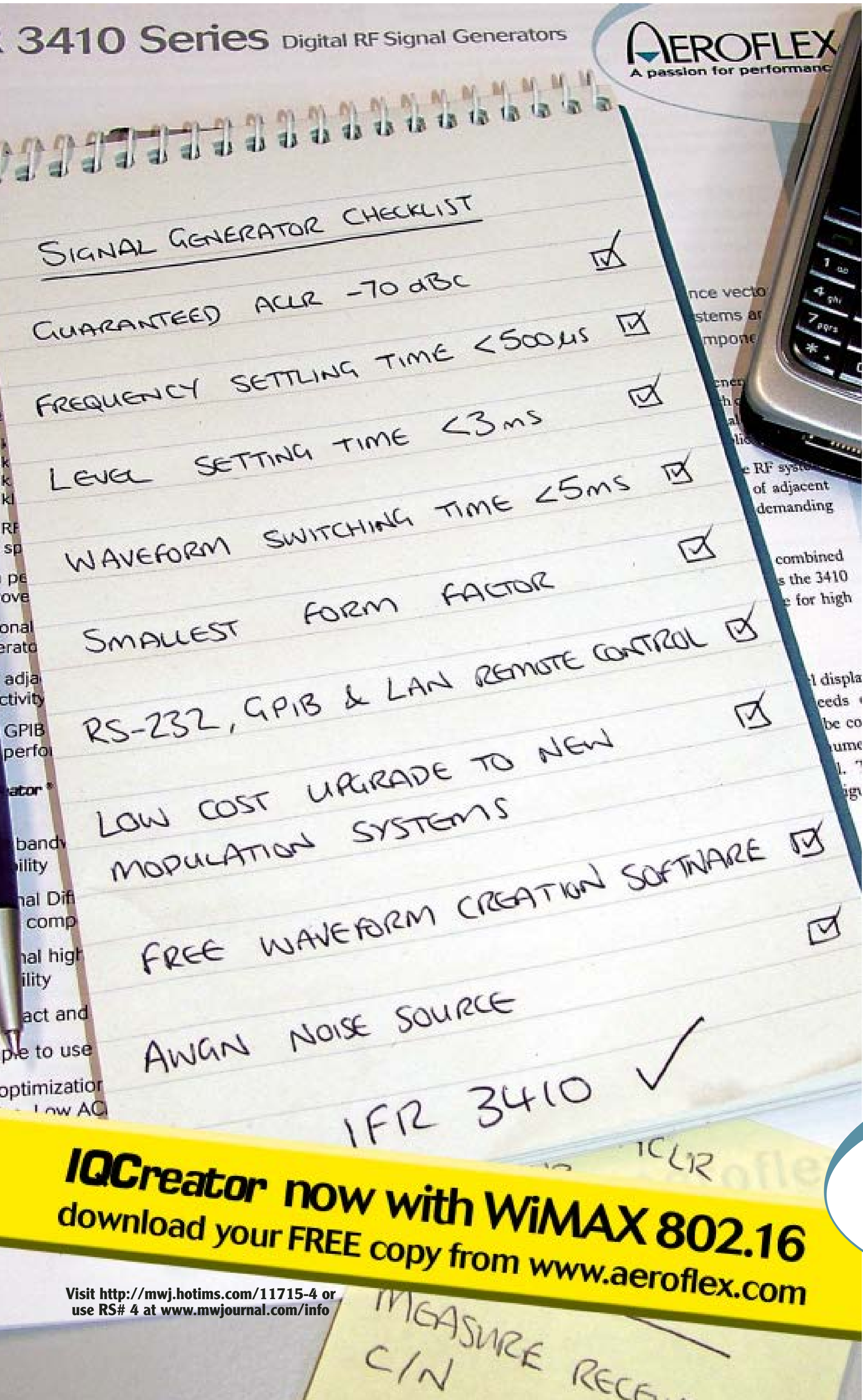

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An alternative approach is the circuit-level linearization technique, based on the derivative superposition method (DSM), which utilizes multiple field effect transistors (FET) of different gate widths and gate biases.[5–7] The DSM applications have been primarily used on MMIC power amplifiers. This technique can be successfully applied to a Doherty amplifier. By comparing it with APD, which is a popular linearization technique, the DSM can achieve good linearity without the requirement of any external circuitry. Doherty amplifiers with improved efficiency and linearity have been reported recently.[8,9] The stringent linearity specifications required for WCDMA repeater or base station applications could not be met without an additional linearization technique. Therefore, the ACLR specifications of the Doherty amplifier require the use of both circuit- and system-level techniques simultaneously. In this article, an optimized 20 W, high power and highly linear, digitally pre-distorted Doherty amplifier, which uses DSM, is proposed. The linearity of the Doherty amplifier is first improved by using the DSM at the circuit-level. Digital pre-distortion is then utilized so that the Doherty amplifier is maximally optimized.

ANALYSIS OF A LINEARIZED DOHERTY AMPLIFIER

Derivative Superposition Structure

Figure 1 shows the configuration of a multiple FET combined amplifier, using the derivative superposition method. The main and N-auxiliary amplifiers are represented by their transconductance stages. The main amplifier is identified as transistor M, which is biased by the gate voltage V_M. The auxiliary amplifier N consists of a transistor M_N, which is biased by the gate voltage V_{gsN}. The gate biases are adjusted to compensate for the nonlinear characteristics of the main transistor.

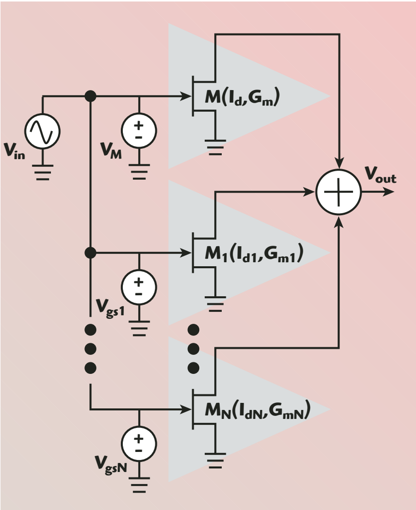


Fig. 1 *Configuration of a multiple FET combined amplifier using the DSM technique.*

The total output current of the multi-FET combination is expressed as

$$I_{out} = M\left(I_d, G_m\right) + M_1\left(I_{d1}, G_{m1}\right) + M_2\left(I_{d2}, G_{m2}\right) + \ldots + M_N\left(I_{dN}, G_{mN}\right) \quad (1)$$

where

G_m = transconductance, controlled by the gate-source bias V_{gs}

The DSM requires the summation of the derivatives of the various FET drain currents with respect to their gate voltages in order to achieve the desired transfer characteristics. The nonlinear transconductance products generated by the main amplifier can be removed by independently compensating with the transconductance of the N-auxiliary amplifiers. This multiple FET amplifier can be applied to the Doherty structure, using two parallel LDMOS FETs. ***Figure 2*** shows the transfer function derivatives of a LDMOS FET model as a function of gate bias voltages. The third-order G3 term, which is of interest in power amplifiers, determines the in-band third-order intermodulation (IM3) distortion products. The G_3 term can be observed to change slope and sign when the mode of operation moves between class AB and class C. In general, LDMOS FETs biased in class AB or class C mode have different transfer function derivatives versus gate bias and input voltage. C. Fager, et al. have demonstrated the LDMOS FET transfer function derivatives for different classes of operation.[10] The transfer function of a LDMOS FET can be modeled by a Taylor series expansion as follows:

$$I_{out}\left(V_{in}(t)\right) = \left.\frac{dI_{DS}}{dV_{GS}}\right|_{V=V_{GS}} V_{in}(t) + \frac{1}{2!}\left.\frac{d^2I_{DS}}{dV_{GS}^2}\right|_{V=V_{GS}} v_{in}^2(t) + \frac{1}{3!}\left.\frac{d^3I_{DS}}{dV_{GS}^3}\right|_{V=V_{GS}} v_{in}^3(t) + \ldots = G_1 \bullet v_{in}(t) + G_2 \bullet v_{in}^2(t) + G_3 \bullet v_{in}^3 \ldots \quad (2)$$

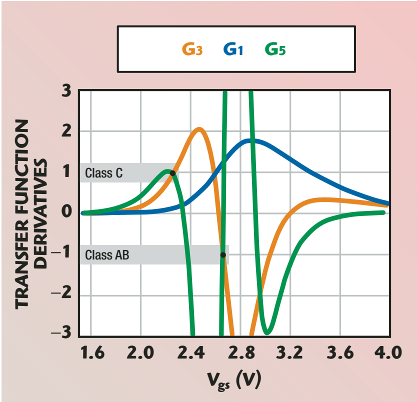


Fig. 2 *Transfer function derivatives of a LDMOS FET model as a function of gate bias.*

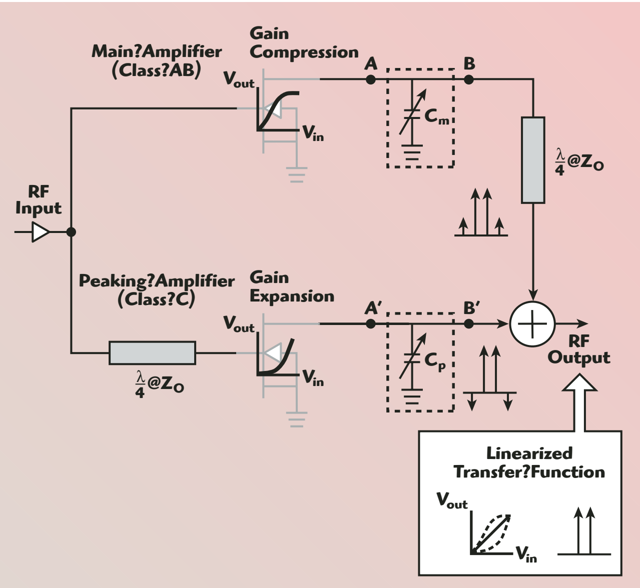


Fig. 3 *Linearization principle of the Doherty amplifier using a DSM structure and shunt.*

where v_{in} is an input voltage and the coefficients G_n are the transfer function derivatives of the nth-order IM products. In the design of a Doherty amplifier, the main amplifier is biased in the class AB mode and the peaking amplifier operates in the class C mode.

Linearization Optimization of the Doherty Amplifier Using Shunt Capacitors

The proposed linearization principle of the Doherty amplifier is shown in ***Figure 3***. The general principle is similar to utilizing the DSM, by adjusting two different gate biases. When the gain compression curve of the main class AB amplifier is compensated by the gain expansion curve of the peaking class C amplifier, a linear transfer function can be obtained. In order to understand the cancellation of the third-order term in the spectral domain, a two-tone input signal is applied

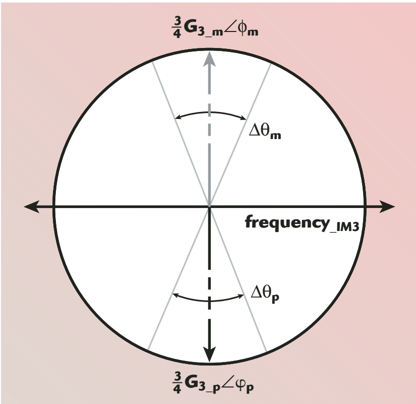
$$V_{in}(t) = A\left[\cos(w_1 t) + \cos(w_2 t)\right] \quad (3)$$

When a two-tone signal is injected into the main and peaking amplifier, the upper and lower sideband third-order IM terms (IM3) generated at the output of the main and peaking amplifiers can be calculated. In the memory-less amplifier model, the upper and lower sideband frequency components are symmetrical; therefore, the focus is on just the upper sideband. Using a Volterra series, the upper sideband third-order IM terms, 2_{w2-w1}, of the main and peaking amplifier outputs at point A and A', in terms of $I_{out(vin)}$, are given by

$$I_{out\_main'}(2w_2 - w_1) = \frac{3}{4} G_{3\_m} \left|A^3 H_m(\omega_1) H_m^2(\omega_2)\right| \cos\left[(2\omega_2 - \omega_1)t + \phi_m\right] \quad (4)$$

$$I_{out\_peak'}(2w_2 - w_1) = \frac{3}{4} G_{3\_p} \left|A^3 H_p(\omega_1) H_p^2(\omega_2)\right| \cos\left[(2\omega_2 - \omega_1)t + \phi_p\right] \quad (5)$$

where H(w) is the nonlinear transfer function and G_{3m} and G_{3p} are the transconductances generated by the main and peaking amplifiers, respectively. Also, ϕ_m and ϕ_p are the phases of the third-order IM terms, which depend on G_{3m} and G_{3p} of the main and peaking amplifiers. The adjustment of the two variable capacitors will result in the phase of the main and peaking amplifier outputs being a function of the frequency and capacitance. This can be respectively writ-



▲ *Fig. 4 Third-order intermodulation linearization of the Doherty amplifier using the shunt capacitors.*

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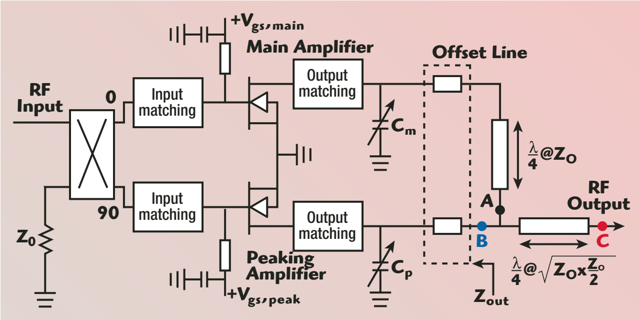

▲ *Fig. 5 Schematic diagram of a highly linear Doherty amplifier.*

ten as

$$\Delta\theta_m = f\left(w, \Delta C_m\right) \quad (6)$$

$$\Delta\theta_P = f\left(w, \Delta C_P\right) \quad (7)$$

Incorporating Equations 6 and 7 into Equations 4 and 5 at point B and B', the IM3 of the main and peaking amplifiers can be simply written as

$$I_{out\_main},\left(2w_2 - w_1\right) = \alpha_{3m}\cos\left[\left(2\omega_2 - \omega_1\right)t + \phi_m + \Delta\theta_m\right] \quad (8)$$

$$I_{out\_peak},\left(2w_2 - w_1\right) = \alpha_{3p}\cos\left[\left(2\omega_2 - \omega_1\right)t + \phi_m + \Delta\theta_p\right] \quad (9)$$

where the IM3 magnitude of the main and peaking amplifiers, α_{3m} and α_{3p}, are

$$\alpha_{3m} = \frac{3}{4}G_{3\_m}\left|A^3H_m\left(\omega_1\right)H_m^2\left(\omega_2\right)\right|,$$

$$\alpha_{3p} = \frac{3}{4}G_{3\_p}\left|A^3H_p\left(\omega_1\right)H_p^2\left(\omega_2\right)\right| \quad (10)$$

In order to reduce the IMD3 term, Equation 11 must be minimized

$$20\log\frac{\left|\alpha_{3m}\right|}{\left|\alpha_{3p}\right|}\angle$$

$$\left|\left(\phi_m + \Delta\theta_m\right) - \left(\phi_p + \Delta\theta_p\right)\right| \quad (11)$$

Accordingly, if the IM3 magnitudes of G_{3m} and G_{3p} are assumed to be the same, then the IM3 phase between the main and peaking amplifiers can be written as

$$\left|\Phi_m + \Delta\theta_m\right| + \left|\phi_p + \Delta\theta_p\right| = \pi \quad (12)$$

Using $\Delta\theta_m$ and $\Delta\theta_p$, the minimum IMD3 can be achieved, as shown in ***Figure 4***. Note that the third-order G_3 terms of the class C biased peaking amplifier have a sign opposite to that of a class AB biased main amplifier. Consequently, after the shunt capacitors values are adjusted, the gate bias of the main and peaking amplifiers and the input voltages could be properly optimized and the third-order IM products generated by the Doherty amplifier should be ideally cancelled out. The two critical parameters, which affect the minimization of the IMD3, include the gate bias and the output shunt capacitors.

DESIGN AND SIMULATION

A 20 W, high power Doherty amplifier is designed by using a push-pull


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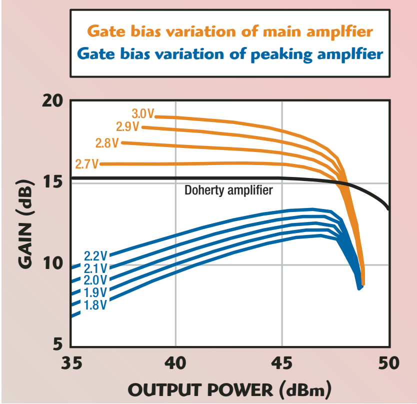
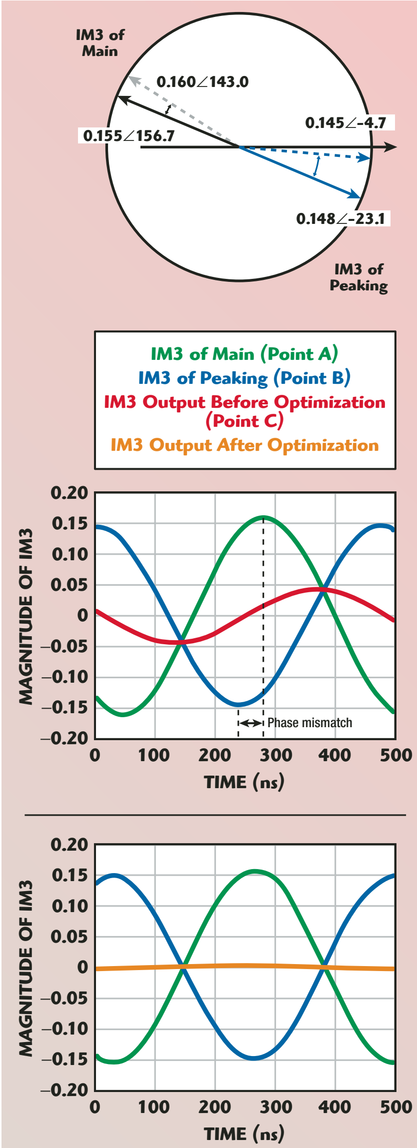
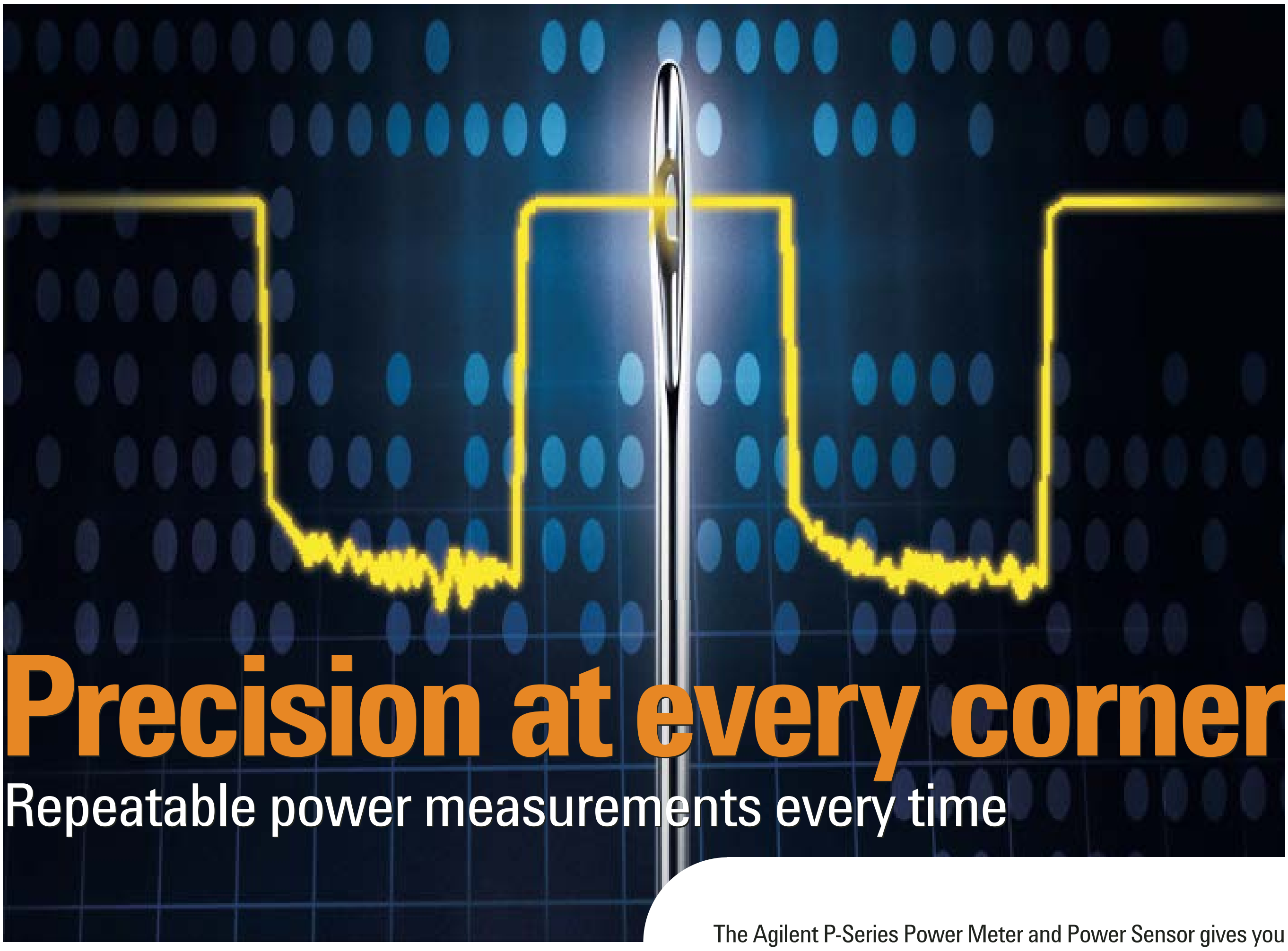
packaged MRF6P21190 (Freescale's LDMOS FET) with a P1dB of 190 W. The simulation of the Doherty circuit was performed using Agilent's ADS software. ***Figure 5*** shows the schematic diagram for the highly linear Doherty amplifier proposed in this article. One device is used as the main amplifier, while the other is the peaking amplifier. A 90° hybrid coupler is used to achieve the –90° phase shift at the peaking amplifier. The peaking compensation lines and shunt capacitors are inserted so that both the efficiency and linearity of the Doherty amplifier are optimized. The output impedance, Z_{out}, of the peaking amplifier was simulated to be 5.4 + j48.8 (Γ_{out} = 0.895 – 91.1°). By inserting the offset line, this point can be moved at 822+j260 (Γ_{out} = 0.895 ∠ 2.0°). Therefore, this corresponds to an optimum high resistance, R_{opt} = 822 Ω. The high impedance of the peaking amplifier enables the output power of the main amplifier to be fully delivered to the load. Thus, the offset line is neces-



▲ *Fig. 6 Simulated gain performance of the Doherty amplifier as a function of bias and output power.*



▲ *Fig. 7 Simulated upper IM3 performance of the Doherty amplifier.*



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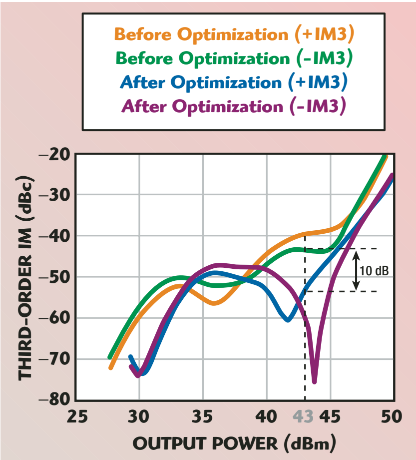
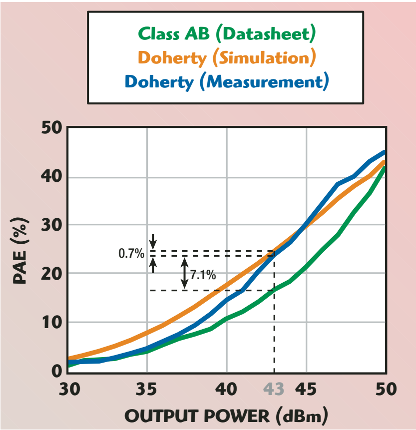
sary to prevent leakage power from the main amplifier into the peaking amplifier. The offset line has been shown to be very sensitive to the overall efficiency and linearity of Doherty amplifier.[4]

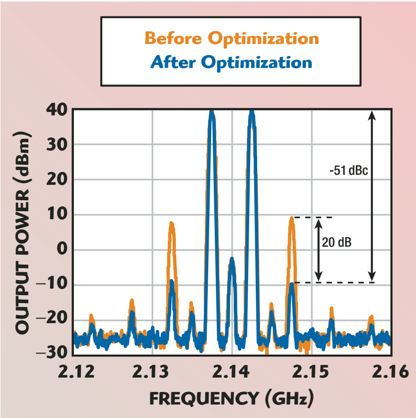
Figure 6 shows the simulated gain performance of the Doherty amplifier as a function of the gate bias of the main and peaking amplifiers. The bias dependent gain expansion characteristics of the peaking amplifier and also the gain compression characteristics of the main amplifier can be observed. The designed Doherty amplifier has gate bias points of 2.88 V for the main amplifier and 2.07 V for the peaking amplifier. ***Figure 7*** shows the simulated upper IM3 performance at points A, B and C. Using shunt capacitors, the phase mismatch between the IM3 of the main amplifier and the IM3 of the peaking amplifier can be removed. The IM3 of 0.160 ∠ 143° for the main amplifier was moved to 0.155 ∠ 156.7° and the IM3 of 0.145 ∠ –4.7° for the peaking amplifier was simultaneously moved to 0.148 ∠ –23.1°. Therefore, the necessary 180° out of phase characteristic for a highly linear Doherty amplifier could be achieved. ***Figure 8*** shows the simulated IM3 performance of a high power Doherty amplifier based on a two-tone input signal. The linearity performance of the Doherty amplifier was optimized using the gate biases, the offset lines and the shunt capacitors. The IM3 performance of the Doherty amplifier, based on the optimization of shunt capacitors, could be improved by 10 dB in comparison to that of the Doherty amplifier before optimization. The corresponding power-added efficiency (PAE) was 24.8 percent at an average 20 W output power at 10 dB back-off.



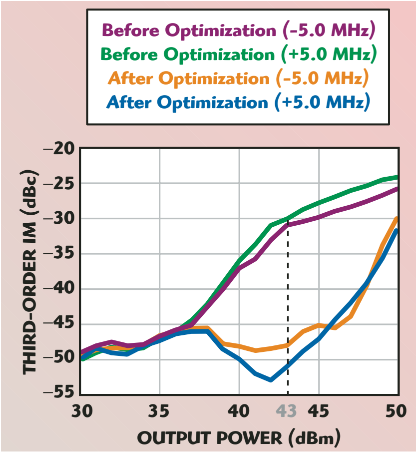
▲ *Fig. 8 Simulated IM3 performance of the high power Doherty amplifier.*



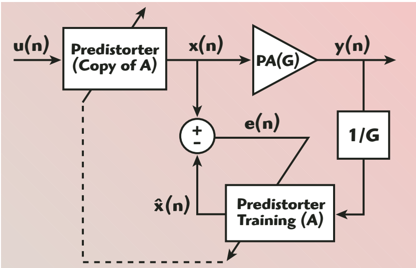
▲ *Fig. 9 Measured PAE of the highly linear Doherty amplifier compared with the simulation and a class AB amplifier.*



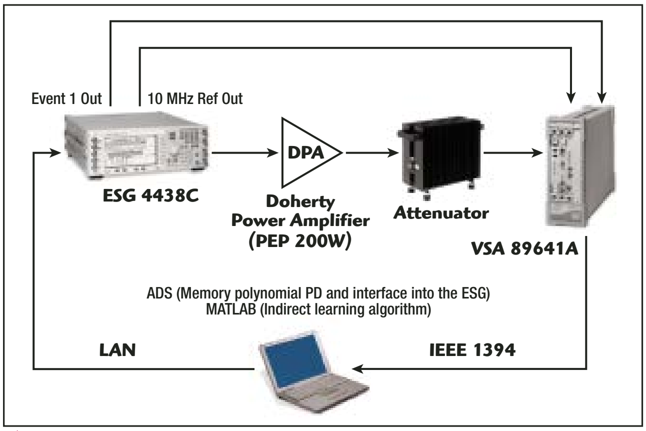
▲ *Fig. 10 Measured IM3 performance of the Doherty amplifier with a two-tone input signal.*



▲ *Fig. 11 Measured IM3 performance of the Doherty amplifier as a function of output power.*



▲ *Fig. 12 Simple structure of an indirect learning algorithm.*



▲ *Fig. 13 Test bench set-up for the measurement of the digitally predistorted Doherty amplifier.*

EXPERIMENTAL RESULTS

A Highly Linear Doherty Amplifier

A highly linear Doherty amplifier, using Freescale's MRF6P21190HR6, was fabricated and measured at a center frequency of 2140 MHz using a single-tone signal, a two-tone signal and a single carrier WCDMA signal with a peak-to-average ratio of 9.8 dB. ***Figure 9*** shows the measured efficiency characteristics of the highly linear Doherty amplifier compared to that of a Class AB amplifier datasheet[11] and the simulated Doherty amplifier. The PAE of the Doherty amplifier could be improved by 7.1 percent compared to that of the Class AB amplifier at an average 20 W output power at 10 dB back-off. ***Figure 10*** shows the measured IM3 performance of the Doherty amplifier based on a two-tone input signal (2137.5 and 2145.5 MHz). Through optimization of the shunt capacitors (C_m = 0.6 pF and C_p = 0.4 pF), the IM3 performance of the Doherty amplifier improved 20 dB in comparison to that of the Doherty amplifier without shunt capacitors.

These shunt capacitors must be selected with small values, which do not affect the matching circuit. At an average power of 43 dBm, the IM3 performance of the optimized Doherty amplifier achieved –51 dBc. At this point, the gate voltages of main and peaking amplifiers were +2.95 and +2.12 V, respectively. ***Figure 11*** shows the IM3 performance of the Doherty amplifier as a function of output power. From the measured results, it is confirmed that an IM3 sweet-spot region with high linearity was obtained using the derivative superposition method in the Doherty structure. The measured results agree well with the simulation results.

Digitally Pre-distorted Doherty Amplifiers

Digital pre-distortion has been applied, using the indirect learning algorithm for a memory polynomial predistorter (PD), as shown in ***Figure 12***. For the memory polynomial PD, the indirect learning using a recursive least square (RLS) algorithm was applied.[12] The coefficients update equation can be expressed as

$$a^{n} = a^{n-1} + K(n)e^{*}(n) \qquad (13)$$

where a is the column vector for coefficients in the memory polynomial predistorter, e(n) is the error signal defined by

$$e(n) = x(n) - y(n)^{T} a^{n-1} \qquad (14)$$

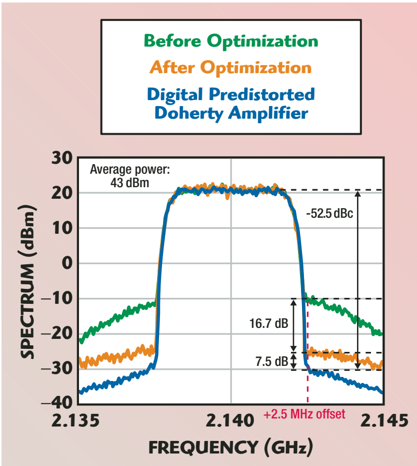
where y(n) is the row vector equal to [y(n) y(n)|y(n)| … y(n–1)|y(n–1)| …], and K(n) is the gain vector defined by

$$K(n) = \frac{P(n-1)y^{*}(n)}{\lambda y^{T}(n)P(n-1)y^{*}(n)} \qquad (15)$$

where λ is the forgetting factor, * represents the complex conjugate and the P(n) is updated as follows

$$P(n) = \frac{P(n-1) - K(n)y^{T}(n)P(n-1)}{\lambda} \qquad (16)$$

Figure 13 shows the test bench set-up of the digitally pre-distorted Doherty amplifier. This test bench consists of a programmable signal generator (ESG E4438C) as a direct up-conversion path, a Doherty power amplifier (DPA), a vector signal analyzer (VSA 89641A) as a digital receiver to collect digital baseband samples from the output of the DPA, and a personal computer for digital



▲ *Fig. 14 Measured WCDMA one-channel spectrum of a Doherty amplifier.*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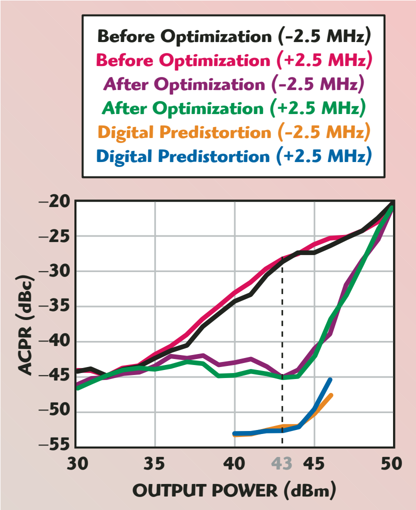
signal processing. In the personal computer, Agilent ADS™ has been used for synchronizing both the samples from the signal analyzer and the samples at the output of the memory polynomial predistorter, that is, the original input for the first iteration, implementing the memory polynomial predistorter, and interfacing with the signal generator and after having both samples time-aligned, the indirect algorithm for parameter extraction has been implemented using Mathworks MATLAB.™

Figure 14 shows the measured WCDMA one-channel spectrum of the Doherty power amplifier with and without the inclusion of shunt capacitors as well as when digital predistortion is applied. At an output power of 20 W, the ACLR of an optimized Doherty amplifier with shunt capacitors improved by 16.7 dB compared to the Doherty amplifier before optimization, at the upper frequency offset of 2.5 MHz. By applying digital pre-distortion, a further ACLR improvement of 7.5 dB was obtained. The resultant WCDMA ACLR performance was –52.5 dBc at a 2.5 MHz frequency offset. The corresponding power-added efficiency was 24 percent. At this point, the gate voltages of the main and peaking amplifier are +2.93 and +2.17 V, respectively. ***Figure 15*** shows the measured ACPR of the Doherty amplifier as function of output power. All the results were measured at ±2.5 MHz frequency offset from a center frequency of 2140 MHz. From the measured results, it is confirmed that the linearity of the Doherty amplifier can be improved by using the proposed optimization methodology.



▲ *Fig. 15 Measured ACPR of the Doherty amplifier as a function of output power.*

CONCLUSION

An enhanced Doherty amplifier with highly optimized linearity using the derivative superposition method was designed and implemented for WCDMA repeater applications. Since DSM is a linearization technique based on the transconductance characteristics, it was found that the gain compression of the main amplifier, biased in class AB, can be compensated by combining it with the gain expansion of the peaking amplifier, biased in class C. In order to achieve IM3 cancellation in the Doherty structure, the gate biases of the main and peaking amplifiers must be optimized. The linearity optimization of the Doherty amplifier can be obtained by adjusting these important parameters: the offset lines, the gate biases and the shunt capacitors. A combination of digital pre-distortion along with the highly linear Doherty amplifier achieved an ACLR of –52.5 dBc at ±2.5 MHz offset frequency for a WCDMA signal. ■

ACKNOWLEDGMENTS

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DESIGNING MODULES FOR CONCURRENCY IN MULTIMEDIA CO-DESIGN

Module designs, and specifically handset power amplifier (PA) and front-end module (FEM) designs, are at a crossroads. Traditionally, the module has been an integration platform for discrete functional blocks enabled by considerable design margin, reasonable size and power constraints, and the luxury of predicted performance from cascaded analysis. Although these issues may not be of concern in many current module designs, they soon will be, because increasing cost, complexity, integration and functionality will drive modules into realms of new design concerns. For years, going back to the Radiation Laboratory days, the majority of the time and effort invested in module design was spent on individual components. Cascaded analysis by hand and then by spreadsheet, with the associated tradeoff among related blocks, left the majority of the module design task to finding either what combinations of individual block parametrics gave the highest yield, or what the various bonding or surface-mount technology (SMT) passive values were for "tuning in" marginal designs. Later, with the advent of easy-to-use electromagnetic (EM) solvers or tools, some post-layout consideration was given to "design" of the module but, in reality, this was and continues to be more of a verification step.

With the explosion of the wireless market, all this is changing. Consumers want more features for the same price, vendors need more performance at a lower price and module designers are being pressured to deliver. With more functionality going into a smaller footprint, the module can no longer be simply an integration platform. As performance requirements become more stringent, there is precious little margin to meet specifications, let alone design so that functional blocks can be merely cascaded; coupling among components must be minimized or even leveraged, if a PA/FEM module is to be successful in the marketplace. Taking advantage of ever-shrinking market windows means that there may be time for a few design paths, but the days of doing iteratively endless module EM designs, followed by yet another printed circuit board (PCB) manufacturing run, are a thing of history.

In this article, a modern module design approach is explored, with emphasis on efficient design flow and effective methodology. The historical approach is reviewed and compared with a newer approach, looking at breaking

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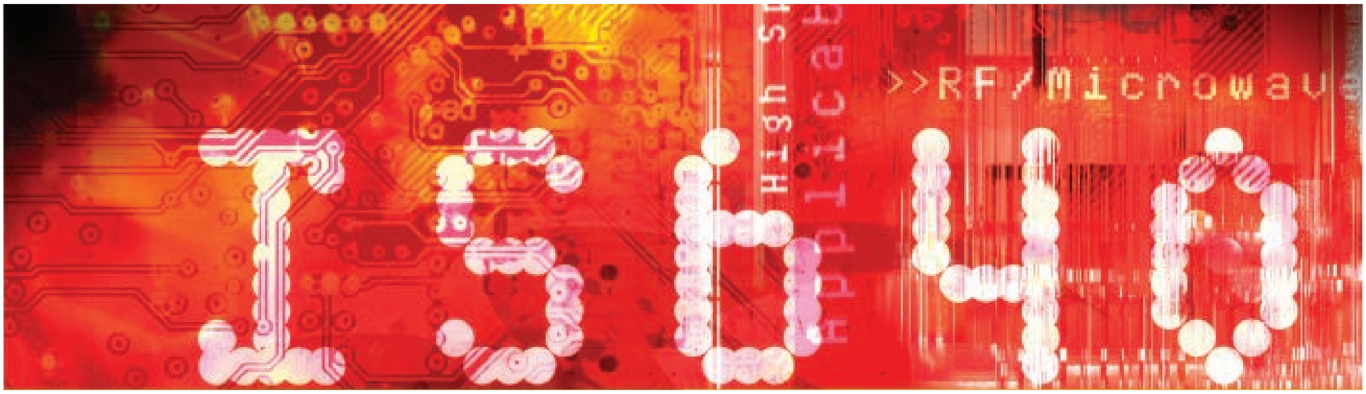

THIN CORE Dk AND Df DATA

Core Thickness	Dk 2, 5 and 10 GHz	Df 2, 5 and 10 GHz
0.0025″	2.83	0.0030
0.0030″	3.07	0.0033
0.0040″	2.90	0.0031
0.0050″	3.37	0.0037
0.0050″	2.83	0.0030
0.0060″	3.49	0.0038
0.0060″	3.07	0.0033
0.0066″	2.95	0.0031
0.0080″	2.90	0.0031
0.0100″	3.37	0.0037
0.0120″	3.49	0.0038
0.0133″	3.31	0.0036
0.0140″	3.26	0.0035
0.0166″	3.52	0.0039
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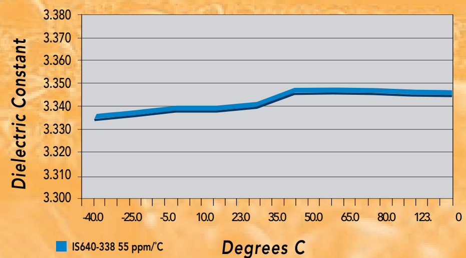
- IS640-338 = Dk 3.38, Df 0.0035
- IS640-333 = Dk 3.33, Df 0.0035
- IS640-325 = Dk 3.25, Df 0.0032
- IS640-320 = Dk 3.20, Df 0.0032
- IS640-300 = Dk 3.00, Df 0.0032
- IS640-280 = Dk 2.80, Df 0.0025

PREPREG DATA

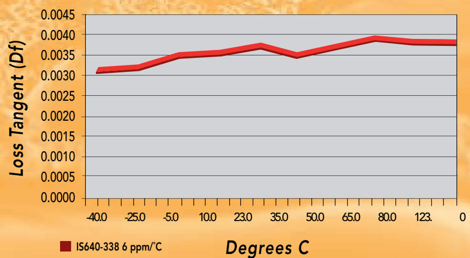
Glass Style	Thickness	Dk 2, 5 and 10 GHz	Df 2, 5 and 10 GHz
106	0.0030″	2.80	0.0028
1080	0.0040″	2.90	0.0031
2113	0.0042″	3.29	0.0036
3070	0.0048″	3.29	0.0035
2116	0.0054″	3.26	0.0035
1652	0.0060″	3.46	0.0038
7628	0.0066″	3.49	0.0038

TCK Dk



Epoxy based systems are at 300 to 400 ppm/°C level

TCK LOSS TANGENT (Df)



Low TCK-Df ppm level very good for Power Handling

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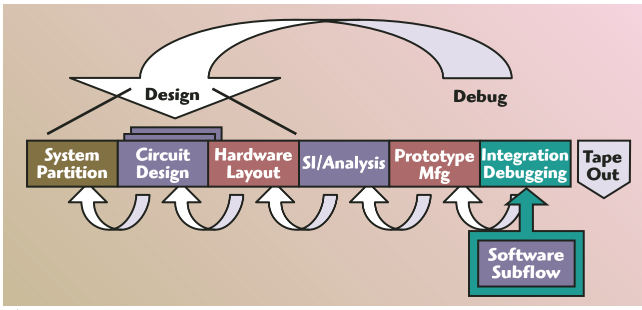
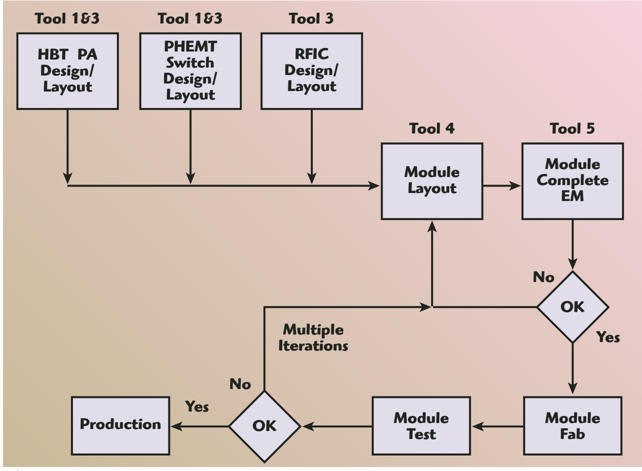
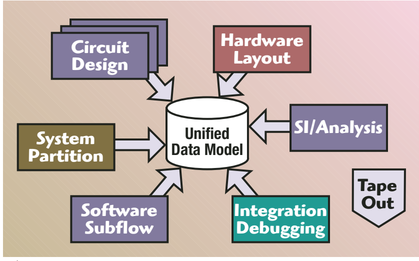


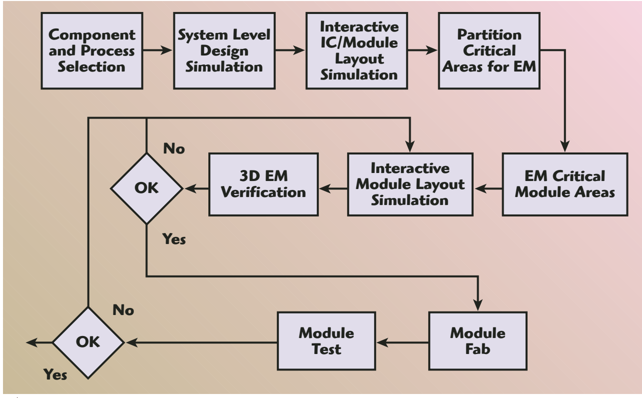
▲ *Fig. 1 Traditional module design flow.*



▲ *Fig. 2 The integration limitations of the traditional EDA software necessitating multiple iterations.*



▲ *Fig. 3 A single database or data model provides accessability to the whole design.*



▲ *Fig. 4 Using a single data model, this flow appears to be serial, but each step is actually concurrent.*

down the previous barriers to actually designing modules by focusing on some very fundamental changes in design: multimedia design, co-simulation and early availability of EM. At a very high level, the flow is the same: partition the design, implement the individual functional blocks, integrate on the module and verify. But this is where the similarity ends, and the overall effect of the new design approach is to provide a higher degree of confidence in less design cycle time, ensuring that the module will be manufacturable in volume, cost-effective and will achieve its market window of opportunity.

DESIGN FLOW OVERVIEW

Traditional Approach

In the design flow used for years to design modules, the flow proceeds very serially, as shown in ***Figure 1***. From system partition to the individual design of multiple components (today normally limited to monolithic microwave integrated circuits (MMIC) or radio frequency ICs (RFIC)), to their layout, etc., electronic design automation (EDA) tools are underlying the flow, supporting pair-wise integration of adjacent steps. This means that while the system and circuit simulation tools may have a translator to share schematics or a way to pass S-parameter files to each other, the circuit tools' integration to layout does not provide a direct or obvious path to system simulation. The databases for the tools supporting any given step are distinct and, therefore, the data representing the design is spread out over multiple tools with no single database encompassing the entire design. Once the many IC components are designed and physically implemented, the module design proceeds. In this subflow, the "design" is actually driven by cramming all of the components into the mechanical outline defining the module package. Module "design" is normally done in a PCB layout tool for this reason, and interconnects consideration is relegated to a secondary, parasitic analysis role rather than a primary design role. On-module components, such as couplers, duplexers, or filters, may be designed using circuit tools, but then they are treated as isolated components similar to the ICs rather than as integrated elements. Within the last 10 years, EM tools have matured substantially, so that the circuit designer can intercept the PCB layout prior to manufacturing and begin tweaking the interconnects to back the design into acceptable performance. The design, as it were, is iterated between moving traces in the PCB, extracting a model for them with EM and simulating this model with behavioral or S-parameter models for the IC in a circuit tool. The ICs are not modified much beyond what their previously portioned performance dictates, except in rare circumstances. Once again, the pair-wise integration limitation of the supporting EDA software dictates that EM is done after layout and layout is done after circuit simulation, as shown in ***Figure 2***.

There is no doubt that EM is an invaluable part of module design. Its proper use provides the most accurate models for the user's design. For modules below 5 GHz or so, the majority of the design is done using RF lumped element design techniques, and the interconnects are better treated as parasitic and extracted rather than primary and modeled (presumably with microstrip or stripline models). However, the EM value in this flow is diminished and limited, because it is not accessible to the circuit designer during design and is used more to limit the parasitic impact of the module as opposed to leveraging the module to the designer's advantage. Furthermore, the same can be said to be true of many

parts of the flow. Individual IC designs are not mutually accessible, so there is limited opportunity to consider cascaded elements until a formal integration. In the case of the traditional flow, this integration is further hampered by the need to sometimes limit the modeling of ICs to S-parameter files and bonding diagrams rather than full, transistor-level descriptions and editable layouts. Opportunities early in the design flow to look at coupling issues, both IC-IC and IC-module, are nonexistent. As such, these can only be dealt with very late in the flow when time is short and re-design options are few.

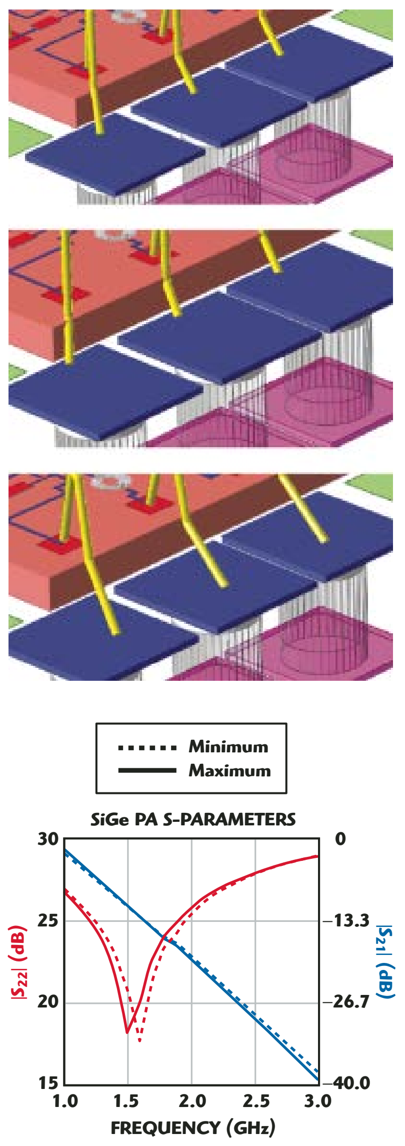
Concurrent Approach

In order to look at coupling issues early in the design flow, it is necessary to reach down into the flow and break the barrier between the circuit designer and the EM solver. At the same time, the same should be done for the system designer. By doing so, concurrency is enabled in the design flow, because all members of the electrical design team have access to the same data through an interface between the tools that support their task in the design flow. Such design flows are said to be concurrent. If this concurrency extends beyond the design media—the same tools and database being used for RFICs, MMICs and modules—the flow is said to be multimedia as well. The key is to create a database or data model for the design that provides accessibility to the whole design for all participants through their step in the process. Furthermore, elements of the design, such as a microstrip, represent a single entry in the data model and each tool accesses the same entry for its use. So notions, such as cross-probing or schematic-driven layout, are no longer features written to integrate a set of tools, but rather are a fundamental consequence of the way the data is stored. Such unifying databases have been implemented in spacecraft design,[1] for example, and have enabled concurrent flows that reduce design time and increase the ability to handle complex designs. Databases of this sort exist for module design and enable a flow, as shown in ***Figure 3***. In this arrangement of tools, it is difficult to see how the flow plays itself out. In a word, it is flexible and can be anything from the arbitrary pinging back-and-forth to the highly serialized arrangement of the traditional approach. A more realistic approach can be seen in ***Figure 4***. The flow appears to be very serial; however, the key difference is that each step is actually very concurrent, as will be discussed later. How would this impact module design? Before the design flow can be considered at a very high level, with a step-by-step approach and seeing the radical effect concurrency can have on cycle time through this change in the module design process, it is important to look at how it changes a critical part of the module flow: the EM solver.

EM IN CONCURRENT DESIGN

In the traditional flow, EM is only available post-layout and is de facto a module design step. This is very late to be using the most accurate means to model critical design elements. Conceptually, it would be desirable to have early access to it. Concurrent flows permit this by primarily removing the data barrier that exists among the tools. Since the layout and the EM are working from the same database, instead of an exported GDSII or DXF file, the EM can be driven directly from layout at any time without having to stop to export a file. The generated model is then automatically placed into the database as one of the possible electrical models for that portion of the design. This creates an interesting dynamic if the way in which the EM analysis is initiated is changed at this point. Imagine a circuit designer whose primary view of the design is the schematic, and now has direct access to the layout. By selecting larger and smaller sections of the layout, or parametrically tuning components—even interconnects—and then initiating the EM analysis through the circuit simulator, the designer has effectively moved EM into the circuit design flow and created a schematic-driven EM capability. The notion of parametric design and a concurrent database enables the designer to go even further. Rather than simply having parametric elements automatically create layout structures, as in the traditional flow's schematic-driven layout, in a concurrent data model these elements could also use highly optimized EM solvers,

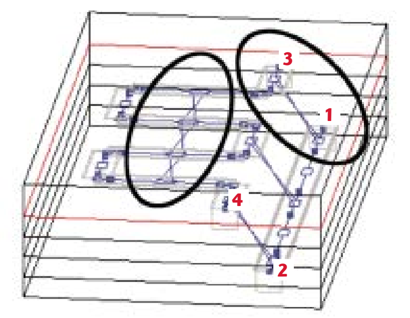
built right into the models, to bring EM into the simulation and provide accessibility during real-time tuning, optimization, or statistical/yield analysis. Other methods rather than an explicit EM solver in the model are also possible.[2] One example is bond wire modeling. Combining the parametric definition of bond wires, including multiple profiles, embedding dielectrics and material parameters, with layout cell generators and specialized EM solvers, three-dimensional (3D) EM simulation of bond wires can be driven by the schematic. This makes EM analysis of module-IC interconnects accessible very early in the design flow, ensuring that it is the same bond wire matrix that is in the layout and is sent to manufacturing. As shown in ***Figure 5***, by parametrically varying the land location of the ground bonds for a silicon germanium (SiGe) PA at 1600 MHz between –50 to +150 µm from the nominal position, it can be seen that the performance shifts without explicit 3D EM. For many interconnect structures, it is desirable to incrementally add parasitic and coupling effects early on, as the design progresses, considering them perhaps as innocuous shorts, then as simple distributed elements and finally as more and more complex coupling arrangements. A new technology available in some software packages offers an intelligent net (iNet) capability, which enables a wire on the schematic to be routed on the layout and modeled using circuit elements.[3] A new EM-like technology, circuit extraction (see ***Figure 6***), can then group together these iNets and instead of doing time-consuming full-wave EM analysis, can effectively create a schematic model using distributed and coupled-line circuit elements. Circuit extract, when combined with EM-based models, brings the design full-circle, having effectively used schematics to kick-off EM, which in turn generates an EM analysis that produces a schematic with embedded-EM.



▲ *Fig. 5 Performance shift without explicit 3D EM when the land location of the ground bonds are varied.*

SYSTEM SIMULATION

The module flow uses system simulation in three areas. Requirements flow-down is used very early in the process to partition the design into functional blocks. Behavioral models represent each component to be designed. Following this, the flow-down can be modified into a module verification mode by swapping out behavioral models for simulation-based ones. These simulation-based models



▲ *Fig. 6 Circuit extraction converts geometry data into distributed models.*

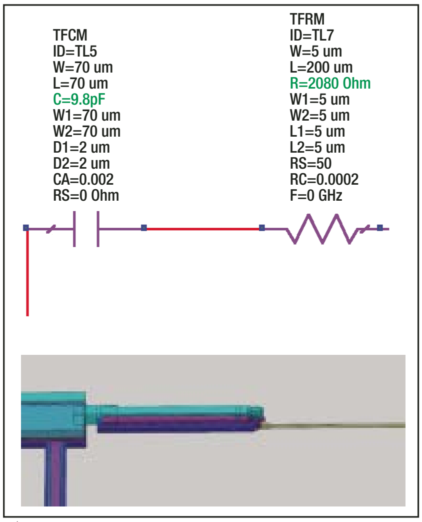
reuse the component schematics at the circuit level and automatically extract the needed system model through the single data model, even to the point that real-time tuning can be used as well as optimization of the system using circuit elements. System simulation can be used in co-simulation with the circuit designs in a fashion similar to the module verification. Individual circuit designs can be inserted into test benches and the circuit schematic can be tuned or optimized for system performance. For a PA module, for example, this could be error vector magnitude (EVM), adjacent channel power ratio (ACPR), or bit error rate (BER).

CIRCUIT DESIGN

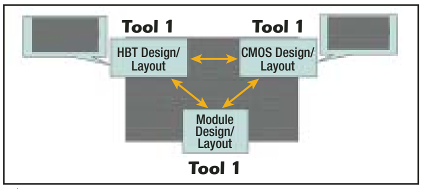
At some level, the designer must start by creating a schematic, doing some simulation and implementing with a little bit of layout. The value in the method under discussion in this article is that all these tasks are in the same tool, sharing the same database and the elements being placed in the schematic instantly have meaning in the other relevant steps in the process. Thus, the manipulation of the design can then switch to the layout, if that is the best way to manipulate the design, with the schematic automatically updating with each and every layout edit. EM can be implemented very early in the flow by using EM-based models or using EM to extract models directly from the layout under schematic control. This can also be done from the layout via the single data model because of the layout-schematic concurrency. This extends also to wires in the schematic. As shown in ***Figure 7***, the wire in the schematic is automatically implemented knowing the precise via type that is needed—the connection to the capacitor is able to discriminate between cap top and bottom and can draw the appropriate via structure. This can then be extracted to circuit models, using circuit extract or S-parameters, using a full-wave EM solver. Because of the ease with which the circuit designer can introduce EM, it is relatively simple to incrementally add more and more peripheral metal to the EM until there is greater certainty of the desired performance. Because this incremental EM is done very early in the flow, it is much easier to make design changes when suggested by the EM results. As previously discussed, this can be done with system co-simulation as well, because the concurrent flow removes the overhead in the traditional flow of extracting behavioral models from the circuit tool and moving them to the system tool.

MODULE-IC CO-DESIGN

Once there is a semblance of a design for each of the components, the designer can now begin taking advantage of the concurrencies across the media. ***Figure 8***, for example, shows that the heterojunction bipolar transistor (HBT) die can be individually designed in a concurrent fashion, as can a complementary metal oxide semiconductor (CMOS) or any other IC technology, in the same toolset, while simultaneously being co-designed with each other and the module itself. The determining factor in where the concurrencies occur is the needs of the design and the creativity and problem solving of the engineer. The primary feature enabling this, beyond the concurrent data model, is the ability to load multiple process design kits (PDKs) for electrical and physical de-



▲ *Fig. 7 Wire automatically implemented for PHEMT design with proper top plate capacitor connections.*



▲ *Fig. 8 An HBT can be designed as well as a CMOS die in a concurrent fashion while being co-designed with each other and the module itself.*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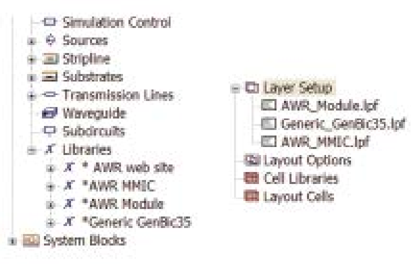
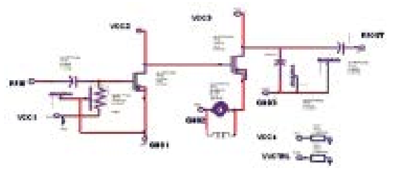
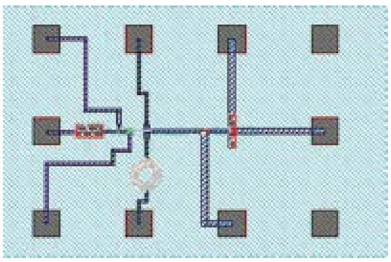
sign. For the example above, this means having multiple layer definitions and library elements for all three of these processes, as shown in ***Figure 9***. Once the multiple PDKs are loaded, different IC-module co-design opportunities can be considered. One obvious area is evaluating the tradeoff between a component on-die or on-module. It can be seen in ***Figure 10*** that the original CMOS PA design calls for an inductor on the source of the second stage. For die cost concerns, the designer may choose to explore moving this inductor, implemented as a spiral in the IC layout, to the module. Taking into account line lengths on the die and the module, as well as the layout-driven bond wire model with built-in EM, a module inductor can be synthesized that gives the equivalent effective inductance on-module as on-die, with a high degree of confidence in the results, as seen in the circled region in ***Figure 11***. Typically, this sort of analysis in the traditional flow would require the use of nearly all the tools (IC layout, PCB layout, circuit simulation and 3D EM), taking hours if not days to coordinate, simulate and analyze for a single iteration of the analysis. Here, in comparison, the whole process takes minutes, including optimizing the module line length. While it is true that as the module is finalized more and more direct current (DC), control and other routed lines will perturb the off-chip inductive solution, the critical design constraints for properly realizing the inductor through the layout-driven bond wire and the parameterized description of the inductive module line have been identified very early in the design process. Good design practices, from this point forward in the flow, will enable the designer to incrementally examine how these other lines perturb the solution. In this way, a warning can be flagged and a second look taken at the module inductor as soon as it becomes an issue. In contrast, in the traditional flow, there would not be any incremental knowledge of this, and the designer would not be able to see which "extra line" tipped the balance, since he/she would only be doing a full-up, complete module EM at the end of the complete, or nearly complete, module layout. Also shown on top of the figure is a large matching inductor for the SiGe PA implemented off the chip. Co-designing this with the IC enables the designer to further minimize die size as well as performing sensitivity analysis for oscillations, before formally completing either the IC or the module design and layout. Once again, all of this is done very early in the flow, before formal or final layout of the module, enabling the SiGe PA designer and the module designer to have a dialog, if not do the outright design, using their preferred tools with a



▲ *Fig. 9 The ability to load multiple PDKs for electrical and physical designs means having multiple layer definitions and library elements.*

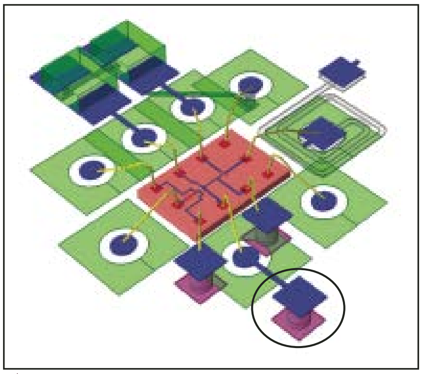


(a)

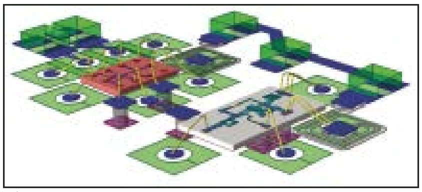


(b)

▲ *Fig. 10 The original CMOS PA design calls for an inductor on the source of the second stage.*



▲ *Fig. 11 A module inductor synthesized, giving an equivalent effective inductor on-module as on-die.*



▲ *Fig. 12 SiGe PA combined with a PHEMT via a coupler.*

single database. This can be extended further to IC-IC co-design. In this mode, the module can be considered immediately, or later on the interconnecting medium. As shown in ***Figure 12***, the subject SiGe PA is now combined with a pseudomorphic high electron mobility transistor (PHEMT) PA via a coupler, presumably for feeding a common, broadband antenna. Once sufficiently designed, the individual die can initially be directly combined or, later at the module level, used to consider the loading of one chip by another. When this is done at the module level, the module interconnect source circuitry on one IC and load circuitry on the other IC become, instead of impediments, opportunities for performance improvement. Thanks to the concurrency in the tools underlying the flow, the performance need not be just circuit, but also system. Complete implementation of the module can proceed once the (transistor-level) elemental descriptions of all the components are added. Co-design across all media boundaries is enabled or, for sufficiently mature and match-insensitive designs, just the module can be considered through design layout and unit verification.

FINAL ANALYSIS AND VERIFICATION

Once the module layout is completed, the designer "pops" back to the top level of the flow and does a final EM analysis and verification at the module level. The EM analysis may be full-module, but more likely than not, it will only be key areas of the module. The identification and partitioning of these areas were identified in the early parts of the IC, IC-module and IC-module-IC co-design segments with the incremental techniques discussed previously. Those areas, flagged as suspect or critical, will be analyzed one more time in this step and then combined with the transistor-level descriptions of the non-EM areas for final circuit- and system-level simulation and yield analysis. Any design rule check (DRC) and layout versus schematic (LVS) are done prior to generating data for IC fabrication, PCB manufacturing and module assembly.

CONCLUSION

Module design is no longer a matter of cascaded S-parameters and PCB layout. Design and market demands are forcing the module design focus to shift from component integration to a co-designed medium. The traditional design flow and underlying design tools are incapable of achieving this within the time-to-market requirements of modern PA/finite element method (FEM) products. Leveraging the lessons of concurrency from other areas, a set of tools and a flow based on a common database provides a low risk path to actually using the module to achieve greater performance, higher yield and lower cost. ■

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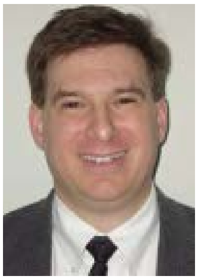

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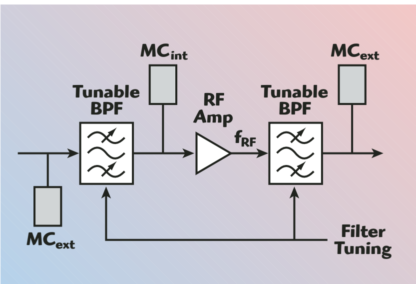
A VARACTOR-TUNABLE FILTER WITH CONSTANT BANDWIDTH AND LOSS COMPENSATION

This article presents the basic concept and realization of a bandpass varactor-tunable filter with constant bandwidth and loss compensation. The filter components are based on step-impedance planar resonators, while the equalizing circuits of L- and T-types are lumped capacitances. The integration of the filter passive parts with a gain block is implemented to compensate for the insertion losses. Examples of practical realizations of two- and four-pole varactor-tunable filters in the 1.1 to 1.5 GHz frequency range are reported.

Varactor-tunable filters attract the attention of microwave specialists due to a number of advantages that can improve the overall performance of communications and radar receivers, as well as measuring equipment. One of the drawbacks of such filters is a considerable variation in bandwidth (BW) and insertion losses (IL) within the tuning range. The problem can be solved by the proper design of equalizing circuits, providing stabilization of these parameters. This article describes the basic concept and realization of such an approach, when the filter components are using step-impedance resonators matched by L- and T-types of equalizing elements. Since implementing additional equalizers leads to increased insertion losses, a gain block, such as an LNA, is integrated with the passive filtering part to compensate for the loss.

Fig. 1 Tunable bandpass filter configuration with external (MC_{ext}) and internal (MC_{int}) equalizers and loss compensation.



BASIC DESIGN CONCEPT

A tunable filter with loss compensation can be constructed by cascading passive tunable filters (or tunable resonators), an RF gain block and external/internal equalizers, as shown in ***Figure 1***. Here, the filtering parts are responsible for creating the needed frequency response, while the gain block compensates for the insertion losses. If the filters (resonators) are tunable (mechanically or electrically) their input/output impedance variations may be considerable, leading to varia-

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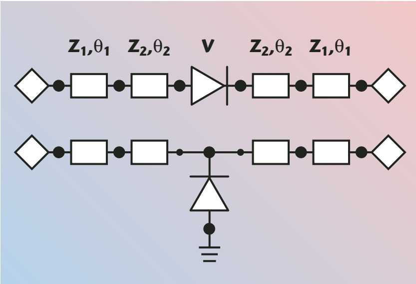
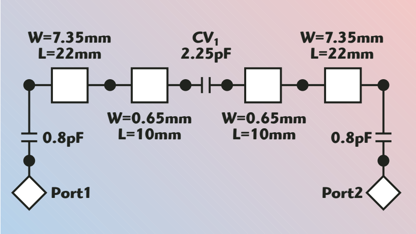
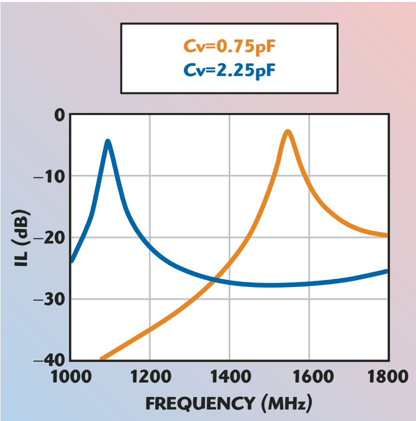


▲ *Fig. 2 Schematics of tunable SIR with the varactor V in series and parallel.*



▲ *Fig. 3 Varactor-tunable SIR with capacitively coupled input/output ports.*



▲ *Fig. 4 Simulated frequency response of the varactor-tunable SIR.*

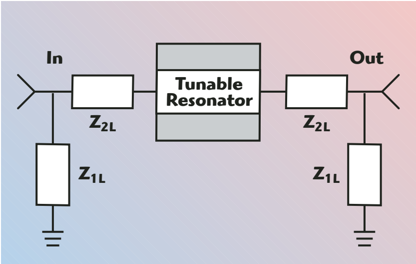
tions of IL and BW within the tuning range. To avoid such an undesirable phenomenon, external and internal equalizing circuits must be added to improve the overall performance. The practical realization of a tunable filter with constant bandwidth and loss compensation (stabilization) requires performing the following basic steps:

- The design of tunable resonators from which the tunable filter is assembled. In this article, step-impedance varactor-tunable resonators will be employed to realize such filtering elements;
- The choice of a configuration of coupling (equalizing) elements providing stabilization of the bandwidth within a specified tuning range. If the filter consists of several resonators, both external and internal equalizers must be determined to provide the best stabilizing effect;
- The choice of the gain block and the design of equalizing elements to minimize the IL variation within the tuning range;
- Integrating all the components into a single assembly, in order to reach the goal: a bandpass varactor-tunable filter with constant IL and BW and loss compensation.

TABLE I

BASIC CHARACTERISTICS OF THE VARACTOR-TUNABLE SIR

Capacitance of varactor CV1 (pF)	0.75 2.25
Resonance frequency (MHz)	1546 1088.7
IL at resonance (dB)	–2.9 –4.2
3 dB bandwidth (MHz)	36.5 23.7
Tuning range (MHz)	450
BW variation (%)	55
IL variation (%)	45

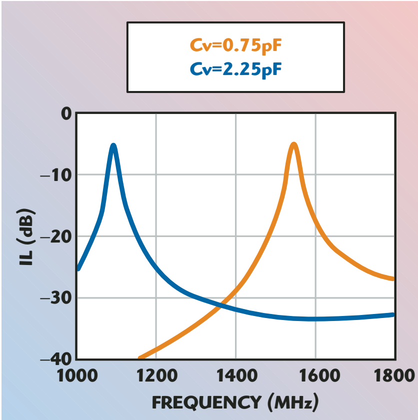


▲ *Fig. 5 Tunable resonator with L-type equalizers at the input and output ports.*

STEP-IMPEDANCE VARACTOR-TUNABLE RESONATORS

Tunable resonators and filters can be realized through a number of methods.[1–5] However, a step-impedance resonator (SIR) is an excellent candidate for creating microwave tunable filters due to some advantages:[6]

- Easy fabrication using planar technology;
- Reasonable manufacturing tolerances;
- Easy integration with varactors and other lumped or distributed components;
- Simple biasing circuitry;
- Wide-range tuning ability (up to 50 percent) with commercially available varactors.



▲ *Fig. 6 Simulated frequency response of the varactor-tunable SIR with input and output equalizers.*

TABLE II

BASIC CHARACTERISTICS OF THE VARACTOR-TUNABLE SIR WITH EQUALIZERS

CV1 (pF)	0.75 2.25
Resonance frequency (MHz)	1544.2 1096.4
IL at resonance (dB)	–4.9 –5.46
3 dB bandwidth (MHz)	23.7 20.5
Tuning range (MHz)	447.8
BW variation (%)	15
IL variation (%)	11

The symmetrical configuration of the SIR, shown in ***Figure 2***, is considered below. It consists of the two lines with different impedances, Z_1 and Z_2 and electrical lengths θ_1 and θ_2, respectively. The varactor diode, used as a tuning element, is placed in the center of the resonator. A more detailed analysis of these configurations[6] showed that the frequency tuning range and mode separation depend on the parameter $\zeta = \theta_1/(\theta_1 + \theta_2)$ as well as the type of coupling element at the input/output ports—capacitive or inductive. The best results are obtained for the parameter ζ = 0.7 to 0.8, assuming $Z_1 = 20\ \Omega$ and $Z_2 = 80\ \Omega$. The SIR with a series varactor demonstrates a higher separation between the principal and nearest higher mode, while its counterpart, with a parallel varactor, has better tunability. Since both SIRs have a symmetry plane with respect to the varactor, only odd (or even) modes

can be tuned while the others are fixed, depending on the position of the varactor-parallel or series. This effect reduces the frequency separation of the resonant modes. However, if the cut-off frequency of the gain block is chosen near the second harmonic, this parameter can be improved in principle. Consider, as an illustration, the varactor-tunable SIR with capacitive input/output couplings shown in ***Figure 3***. The varactor (capacitor CV1 with Q = 100 at 1 GHz) is connected in series and its capacitance varies in the range 0.75 to 2.25 pF, depending on the applied bias voltage. The biasing circuitry is not shown for simplicity.

The SIR is assumed to be fabricated on a Duroid RO-3006 substrate: $\varepsilon_r = 6.15$, $\tan\delta = 0.001$, thickness H = 1.28 mm and a conductor thickness T = 0.035 mm. For these parameters, $Z_1 = 19.9\ \Omega$, $Z_2 = 80\ \Omega$, $\theta_1 = 60°$ and $\theta_2 = 24.3°$, resulting in the parameter $\zeta = 0.71$. The other schematic elements are indicated in the figure, assuming that the capacitors Q = 100. The IL was simulated using the Ansoft Designer SV-2.2[8] circuit simulator for two capacitances of the varactor CV_1 = 0.75 and 2.25 pF (see ***Figure 4***). The other characteristics of this tunable resonator are given in ***Table 1***. It is clear that the variations of bandwidth and insertion loss are not acceptable and need the stabilization discussed below.

STABILIZATION OF BW AND IL

When it is necessary to stabilize BW and IL within a tuning range, the following factors should be taken into account:

- Frequency dispersion of the constitutive characteristics of the substrate, namely ε_r and $\tan\delta$;
- Frequency dispersion of the parameters of both lumped and distributed elements of the filter, responsible for its frequency performance;
- Frequency behavior of the coupling coefficients of the input/output and inter-resonator coupling elements.

The roles of these factors and their real contributions in degrading the filter performance depend on the operating frequency. However, in many practical situations, the coupling elements are the most essential factors leading to variations of BW and IL. A variety of equalizing circuits can be employed to stabilize BW, but only simple capacitive L and T configurations are considered, which can be easily integrated with planar technology.

SINGLE-TUNABLE RESONATOR

A single-tunable resonator with L-type equalizing circuits at the input/output ports is shown in ***Figure 5***. Assuming that the transmission matrix ABCD of a tunable resonator $|T_r|$ is known, the transmission matrix of the tunable resonator with equalizers $|T_{re}|$ can be written as

$$|T_{re}| = |T_e^{in}| \times |T_r| \times |T_e^{out}| \tag{1}$$

where $|T_e^{in}|$ and $|T_e^{out}|$ are the transmission matrices of the input and output equalizers consisting of reactances Z_{1L} and Z_{2L}

$$|T_e^{in}| = \begin{vmatrix} 1 & Z_{1L} \\ \dfrac{1}{Z_{2L}} & 1 + \dfrac{Z_{1L}}{Z_{2L}} \end{vmatrix}$$

and

$$|T_e^{out}| = \begin{vmatrix} 1 + \dfrac{Z_{1L}}{Z_{2L}} & Z_{1L} \\ \dfrac{1}{Z_{2L}} & 1 \end{vmatrix} \tag{2}$$

After multiplying the matrices in Equation 1, the elements of $|T_{re}|$ are determined as

$$A_{re} = \left[\frac{A_r}{Z_{2L}} + (1+q)C_r\right] Z_{1L} + \frac{B_r}{Z_{2L}} + A_r(1+q) \tag{3}$$

$$B_{re} = C_r Z_{1L}^2 + 2Z_{1L}A_r + B_r \tag{4}$$

$$C_{re} = (1+q)^2 C_r + \frac{2A_r(1+q)}{Z_{2L}} + \frac{B_r}{Z_{2L}^2} \tag{5}$$

$$D_{re} = A_{re} \tag{6}$$

where A_r, B_r, C_r and D_r are elements of the transmission matrix of the tunable resonator.[6] Assuming a symmetry with respect of the input and output ports results in $A_r = D_r$; $q = Z_{1L}/Z_{2L}$. By transforming the ABCD matrix into a scattering matrix,[7] with a system impedance Z_0, S_{21} can be written as

$$S_{21} = \frac{2}{2A_{re} + B_{re}/Z_0 + C_{re}Z_0} \tag{7}$$

or

$$S_{21} = \frac{2}{2\left(\dfrac{Z_{1L}}{Z_{2L}} + t + \dfrac{Z_{1L}}{Z_0} + \dfrac{tZ_0}{Z_{2L}}\right)A_{re} + 2tC_{re}Z_{1L} + \dfrac{2B_{re}}{Z_{2L}} + \dfrac{C_r Z_1^2 + B_{re}}{Z_0} + \left(t^2 C_{re} + \dfrac{B_r}{Z_2^2}\right)Z_0} \tag{8}$$

where t = 1 + q. The insertion loss expression, $IL = -20 \log|S_{21}|$, can now be used for optimizing the tunable filter's frequency response within a specified tuning range. The equalizing reactances Z_{1L} and Z_{2L} are considered now as independent variables satisfying the two criteria:

a) minimum variation of insertion loss;

b) minimum variation of bandwidth.

To simplify the minimization procedure to reach the goal, the capacitive elements, $Z_{1L} = 1/j2\pi fC_{1L}$ and $Z_{2L} = 1/j2\pi fC_{2L}$ are tried, so that the following error function ER can be introduced

$$ER(C_{1L}, C_{2L}) = t_1 \left| \frac{IL(C_{1L}, C_{2L})_{V_1} - IL(C_{1L}, C_{2L})_{V_2}}{IL(C_{1L}, C_{2L})_{V_1}} \right| + t_2 \left| \frac{BW(C_{1L}, C_{2L})_{V_1} - BW(C_{1L}, C_{2L})_{V_2}}{BW(C_{1L}, C_{2L})_{V_1}} \right| \tag{9}$$

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▲HFCN-5050+	5500-10000	4200	2.99		•
▲HFCN-5500+	6000-11500	4500	2.99		
▲HFCN-7150+	7900-11000	6150	2.99		
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LFCN-105+	DC-105	250	3.99			•		
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LFCN-160+	DC-160	330	2.99					
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LFCN-3000+	DC-3000	4550	1.99					•
LFCN-3800+	DC-3900	6000	2.99					•
LFCN-4400+	DC-4400	6700	2.99					•
LFCN-5000+	DC-5000	6850	1.99		•		•	•
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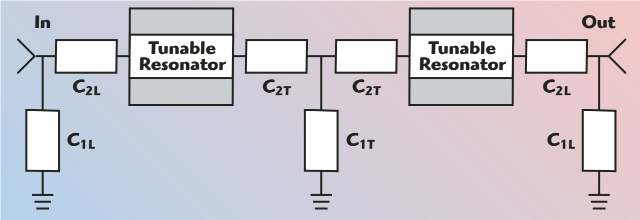
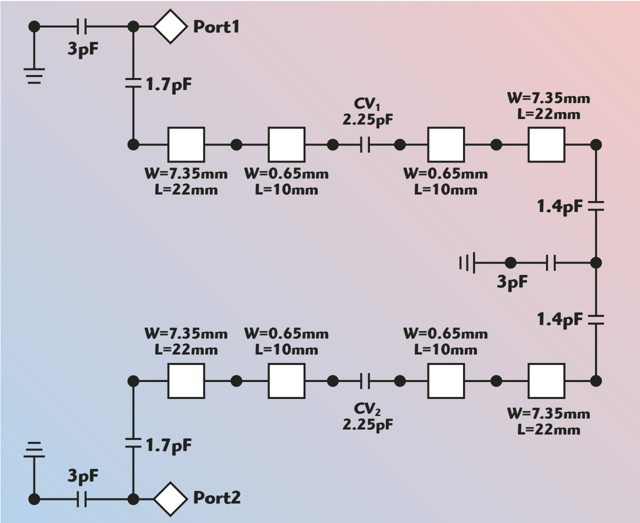
LFCN-5850+	DC-5850	7600	1.99					
LFCN-6000+	DC-6000	8500	1.99		•		•	•
LFCN-6400+	DC-5400	8300	1.99					
LFCN-6700+	DC-6700	9300	1.99		•		•	•
LFCN-7200+	DC-7200	9500	1.99					
			Total number of units in kit:	35	60	55	90	65

LFCN Models: U.S. Patent 6,943,646 except LFCN-800+, -1325+, -2000+ & -2400+.



▲ *Fig. 7 Tunable two-pole filter with L-type equalizers at the input/output ports and an inter-resonator T-type equalizer.*



▲ *Fig. 8 Schematic of a tunable two-pole filter with L- and T-type equalizers.*

where t_1 and t_2 are weighting coefficients ($t_1 + t_2 = 1$) and V_1 and V_2 are the varactor biasing voltages corresponding to the specified tuning range of the resonator. A search for a minimum of the error function (the details are omitted due to space limitation) results in the value of the equalizing capacitors of $C_{1L} \approx 2.2$pF and $C_{2L} \approx 1$pF. The simulated frequency responses obtained for these equalizers are shown in ***Figure 6***, with the same varactor's capacitors values as before.

A comparison of both responses demonstrates that the stabilizations of IL and BW are successful, namely the BW variation is reduced by more than three times and the IL variation is reduced by approximately five times. ***Table 2*** summarizes the results of the above optimization.

COUPLED-TUNABLE RESONATORS

Coupled-tunable resonators, with a T-type capacitive equalizing circuit as an inter-coupling element, are shown in ***Figure 7***. Assuming that the transmission matrix ABCD of a single-tunable resonator $|T_r|$ is known, the transmission matrix of the coupled-tunable resonator with external and internal equalizers $|T_{re}|$ can be written using the same approach as described above for the single-tunable resonator. However, the error function must now be modified to include the parameters of the inter-coupling elements of the T-equalizer, C_{1T} and C_{2T}. It can be written as

$$\mathrm{ER}(C_{1L}, C_{2L}, C_{1T}, C_{2T}) = t_1 \left| \frac{\mathrm{IL}(C_{1L}, C_{2L}, C_{1T}, C_{2T})_{V_1} - \mathrm{IL}(C_{1L}, C_{2L}, C_{1T}, C_{2T})_{V_2}}{\mathrm{IL}(C_{1L}, C_{2L}, C_{1T}, C_{2T})_{V_1}} \right| + t_2 \left| \frac{\mathrm{BW}(C_{1L}, C_{2L}, C_{1T}, C_{2T})_{V_1} - \mathrm{BW}(C_{1L}, C_{2L}, C_{1T}, C_{2T})_{V_2}}{\mathrm{BW}(C_{1L}, C_{2L}, C_{1T}, C_{2T})_{V_1}} \right| \quad (10)$$

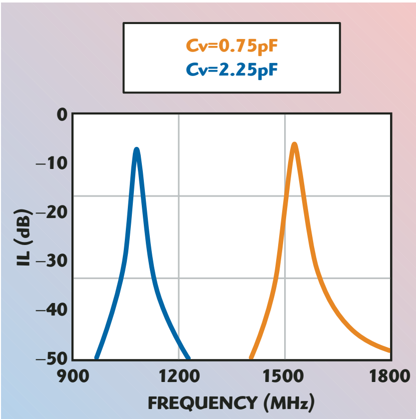
By optimizing the error function, the values of the equalizing capacitors have been determined to be

$$C_{1T} = 3 \text{ pF}, C_{2T} = 1.4 \text{ pF}, C_{1L} = 3 \text{ pF and } C_{2L} = 1.7 \text{ pF}$$

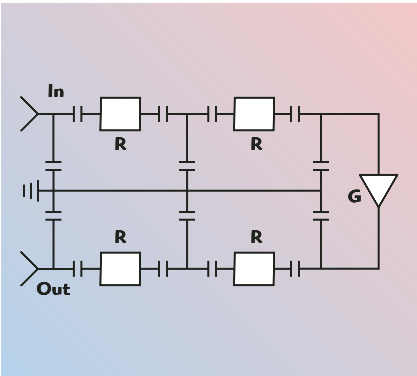
The schematic of the equalized two-pole filter is shown in ***Figure 8*** and its simulated frequency responses are shown in ***Figure 9*** for CV_1 and CV_2 varying in the range 0.75 to 2.25 pF. The BW varies from 18 to 22 MHz and the variation of IL is 6 to 7 dB, within the tuning range 1.08 to 1.53 GHz. However, this level of insertion loss is unacceptable for many applications. To compensate for the insertion losses, a gain block is added between the two-pole tunable filters, as shown in ***Figure 10***. It should be pointed out that implementing the gain block may require a correction of its gain slope within the specified tuning range in order to obtain a flatter IL.

FABRICATION AND TESTING

In order to verify the suggested concept and the results of the nonlinear optimization of the error functions (Equations 9 and 10), varactor-tunable filters were fabricated using planar microstrips on Duroid RO-3006 substrates, SMA connectors and the step-impedance topology previously described. Abrupt junction tuning varactors SMV1405 from Skyworks Solutions Inc. were employed with a biasing circuit providing 0 to 15 V. A photograph of the two-pole tunable filter is shown in ***Figure 11***. The measured IL of this filter is shown in ***Figure 12***. Its tuning range is from 1.0 to 1.4 GHz, its 3 dB BW = 60 ±5 MHz and its IL = 3.5 to 5.0 dB. A four-pole tunable filter has been assembled, using two identical two-pole tunable filters, with a gain block between them. The Mini-Circuits LNA-ZFL1000LN with a gain of approximately 20 dB was integrated within these filters for loss compensation.



▲ *Fig. 9 Simulated frequency response of the two-pole varactor-tunable SIR filter.*



▲ *Fig. 10 Four-pole tunable filter configuration with L- and T-type equalizers, varactor-tunable SIRs (R) and gain block (G).*

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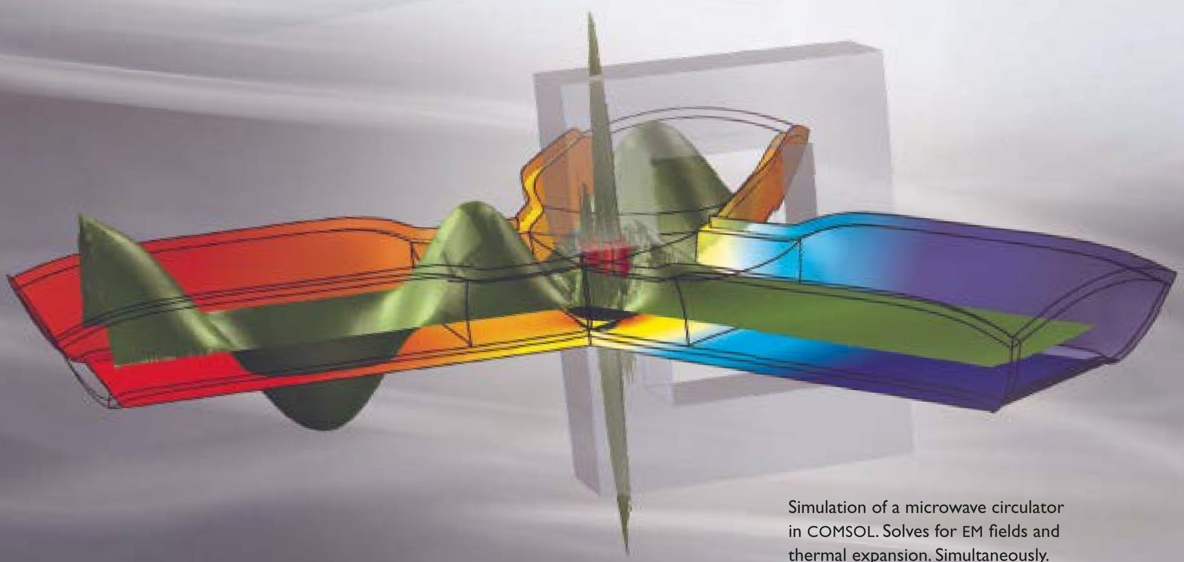

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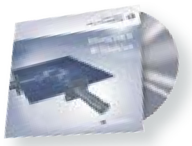

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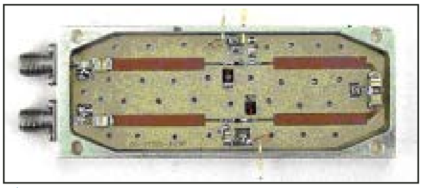
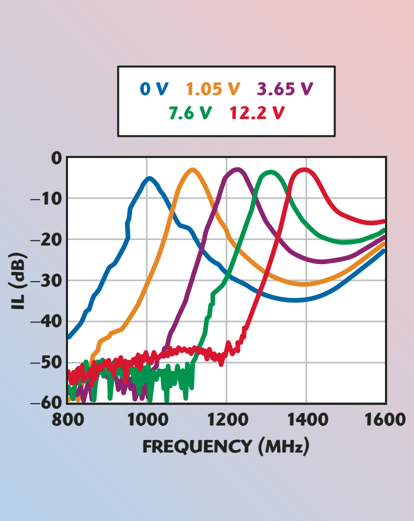
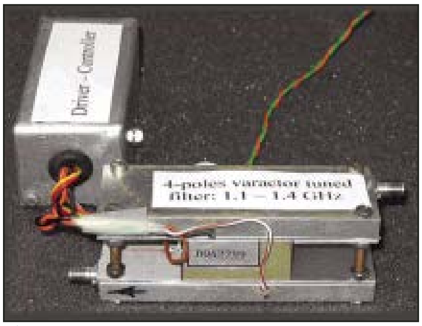


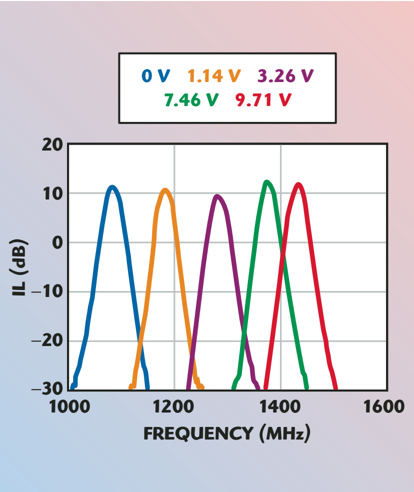
▲ *Fig. 11 The two-pole tunable filter.*



▲ *Fig. 12 Measured insertion loss of the two-pole SIR filter.*



▲ *Fig. 13 The four-pole varactor-tunable SIR filter with its controller-driver.*



▲ *Fig. 14 Measured insertion loss of the four-pole tunable SIR filter with a gain block compensation.*

TABLE III
PERFORMANCE OF THE FOUR-POLE VARACTOR-TUNABLE SIR FILTER WITH LOSS COMPENSATION

Tuning range (MHz)	1080 to 1440
Insertion loss (gain) (dB)	+10 ±1.5
Response type	maximally flat
VSWR	1.5
Number of resonators	4
Number of varactors	4
Connectors	SMA, 50 Ω
DC power supply	15 V/100 mA
Tuning time	depends on the type of driver
Dimensions (mm)	105 × 32 × 32

A photograph of the whole assembly is shown in ***Figure 13***. A special controller-driver has been designed to distribute the biasing voltages between the four varactors from a single DC power supply. ***Figure 14*** shows the measured IL for different biasing voltages. ***Table 3*** summaries the performance of the fabricated four-pole tunable filter.

CONCLUSION

Varactor-tunable bandpass filters based on SIRs have been presented in this article. The major limiting factors such as variation of BW and IL were overcome by using L- and T-types of equalizers. Almost constant BW and IL over the 40 percent tuning range have been achieved with varactor diodes available in the market today. The filters are easy to fabricate using planar microstrip technology suitable for mass-production. ■

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THE DESIGN OF A BAND-REJECTED CROSS SEMI-ELLIPTIC MONOPOLE ANTENNA FOR UWB APPLICATIONS

A cross semi-elliptic monopole antenna with a band-rejected characteristic is presented and investigated. By embedding four L-shaped slits on the cross semi-elliptic monopole, an antenna with a rejected band from 5.29 to 6.20 GHz can be implemented. The good dipole-like radiation characteristics of the constructed prototype are shown. The broadband bandwidth and good radiation properties of the proposed design make it suitable for wireless applications when a rejected band is needed.

Planar monopole antennas, with their advantages of low cost and wideband characteristics, are widely used in wireless applications.[1] However, they suffer from distortion of the radiation pattern at higher operating frequencies, which leads to a directional radiation.[2,3] A cross monopole antenna has been implemented to overcome the pattern distortion at higher operating frequencies. A cross-planar monopole, with an omni-directional radiation in the horizontal plane and a wide operating impedance bandwidth, has been described.[2] A cross semi-circular monopole has also been proposed,[3] but without a rejected frequency band. The interference between the UWB and WLAN systems is an important issue[4,5,6] for UWB applications. The demand for band-rejected characteristics of an antenna is rapidly increasing and some studies of band-rejected cross monopole antennas have been published. A dual-frequency cross-shaped monopole[4] was constructed and investigated. Its band-rejected property in the undesired frequency band was observed. Crossed planar monopole antennas[5] with single and multiple U slots were also implemented. There are two major techniques to reject a frequency band in cross monopole antennas: One is by using slots, the other by using slits. A broadband UWB antenna, using a cross semi-elliptic monopole with a finite ground plane, was successfully achieved.[7] The bandwidth obtained was from approximately 1.85 to more than 12 GHz and a good radiation property was shown. By adding four narrow slits, a 5.25 to 6.40 GHz rejected frequency band was created.

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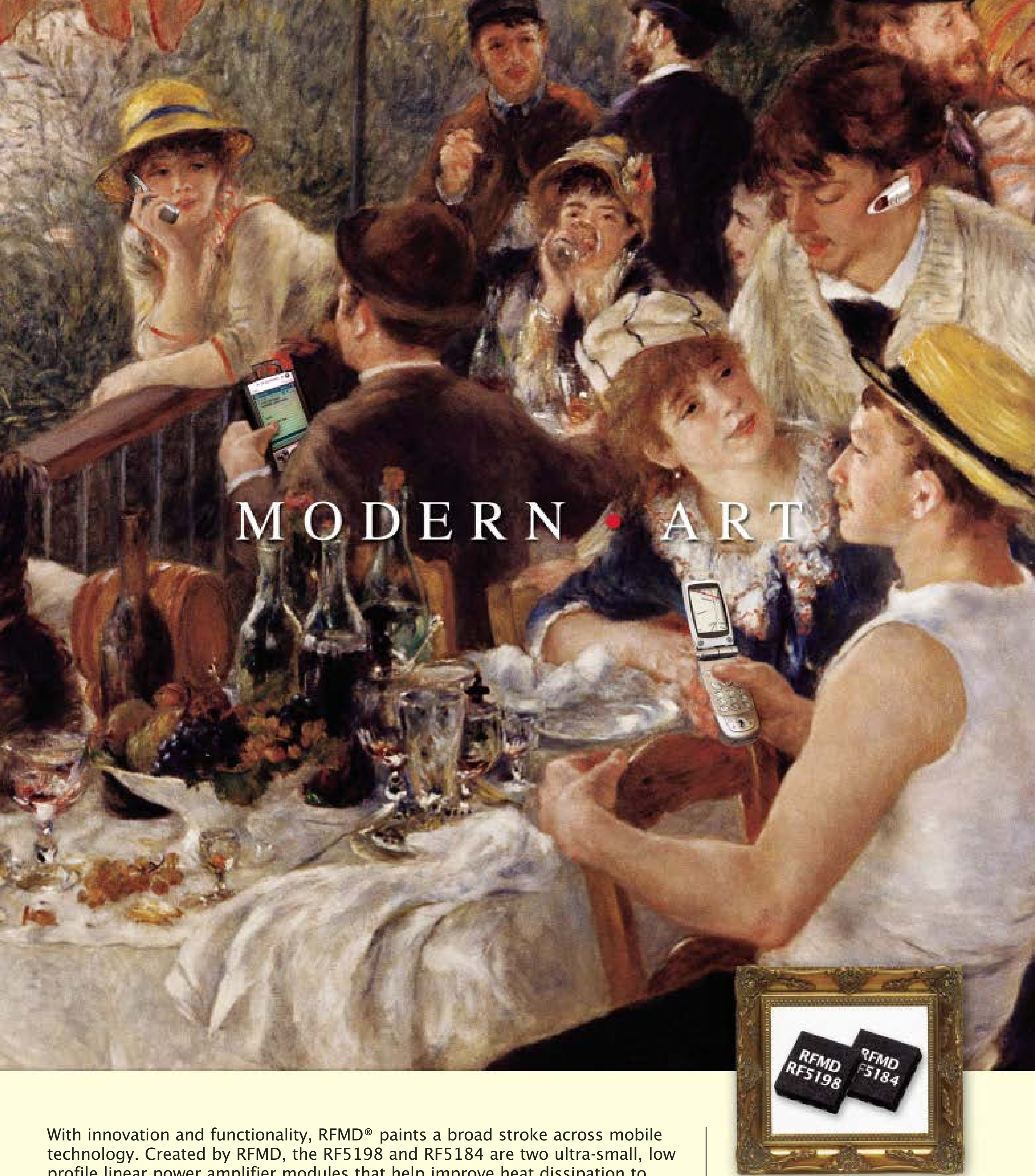

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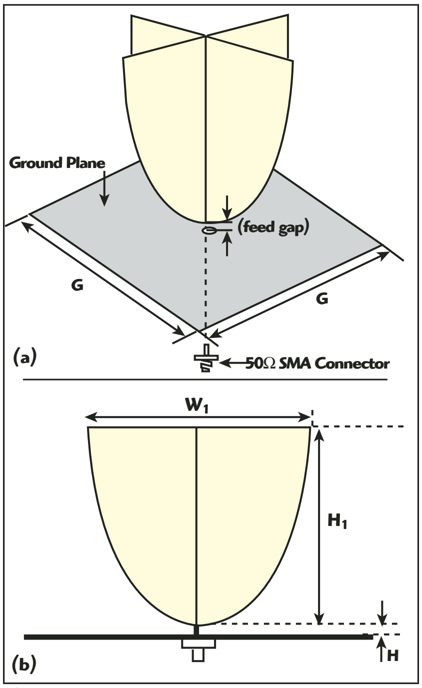
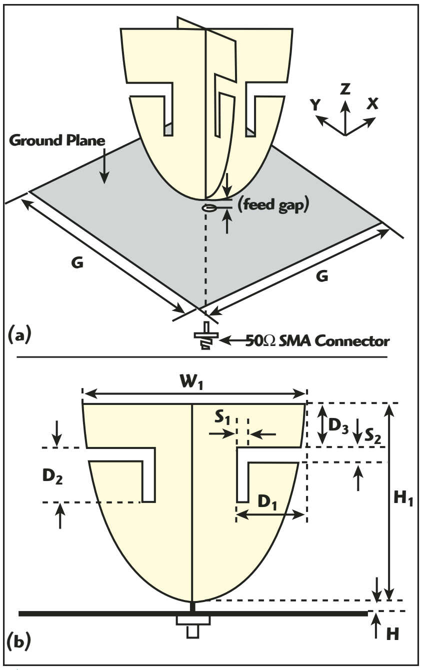
In this article, a novel design of a cross-shaped semi-elliptic monopole antenna with a rejected band is presented and investigated. The band-rejected property is obtained by embedding four L-shaped slits into the lobes of the antenna. The characteristics of the proposed antenna are compared to the cross semi-elliptic monopole antenna with four narrow slits and the crossed planar monopole antennas with single and multiple U slots.[5]



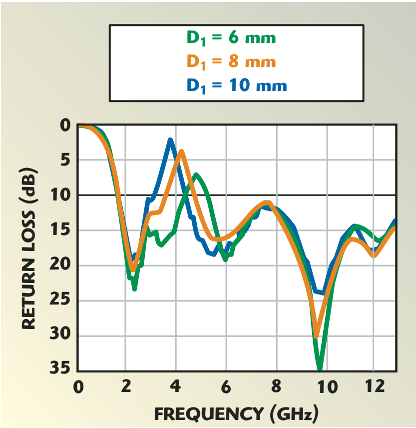
▲ *Fig. 1 Geometry of the cross semi-elliptic monopole antenna; (a) 3D view and (b) side view.*



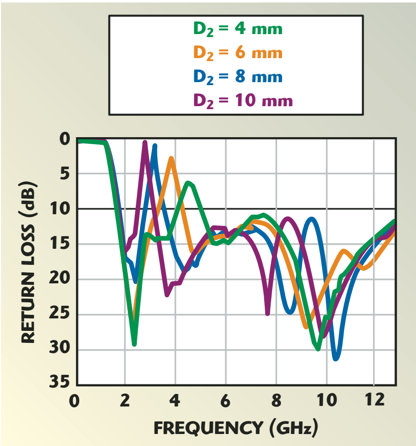
▲ *Fig. 2 Geometry of the band-rejected cross semi-elliptic monopole antenna; (a) 3D view and (b) side view.*

ANTENNA DESIGN

Figure 1 shows the geometry of the cross semi-elliptic disc monopole antenna. The cross monopole is made of 0.1 mm copper sheets, with two semi-elliptic conducting plates located orthogonally above a square ground plane of dimensions G × G × 0.1 mm. The length of the major axis is $2H_1$ and the length of the minor axis is W_1, as shown. The design rules and measured results for this antenna have been published previously.[7] The configuration of the new, band-rejected, cross semi-elliptic monopole antenna is shown in ***Figure 2***. The four L-shaped slits of approximate length $D_2 + D_1$ and width $S_2 = S_1 = 2$ mm are symmetrically embedded into the cross semi-elliptic disc monopole antenna. The cross semi-elliptic monopole is composed of four lobes, which are located in the planes along the x- and y-axes. The ground plane, located in the x-y plane, has the dimensions 120 × 120 × 0.1 mm. When the four L-shaped slits are embedded in the cross semi-elliptic disc monopole antenna, they strongly disturb the current distribution in the specified rejected frequency band. This results in the band-reject characteristics of the antenna. Since most of the current tends to be concentrated near the curved edge of the lobes of the antenna, the location of the slits, used in the proposed band-rejected technique, will be optimum. The current distribution of this design is more effectively disturbed than that of the finite ground plane cross semi-elliptic monopole antenna with four narrow slits.[7] The effect of this strong disturbance is shown in the antenna gain. The overall length of the proposed narrow slit is approximately equal to $(D_1 + D_2) - (S_1 + S_2)$ or approximately 0.22 λc, where λc is the wavelength at the center frequency of the rejected band. The center frequency is a strong function of the overall length of the slit. The bandwidth of the rejected band is determined by the position of the L-shaped slits. In addition, compared to the cross semi-elliptic monopole antenna with four narrow slits,[7] the proposed design has a better gain suppression because the L-shaped slits disturb the current distribution more strongly.



▲ *Fig. 3 Measured return loss for different lengths of D_1.*



▲ *Fig.4 Measured return loss for different lengths of D_2.*

PARAMETRIC STUDIES AND DISCUSSION

The parametric study of the proposed antenna offers some helpful information to antenna engineers. The parameters considered include D_1, D_2 and D_3. Through these investigations, an antenna for UWB application can easily be designed.

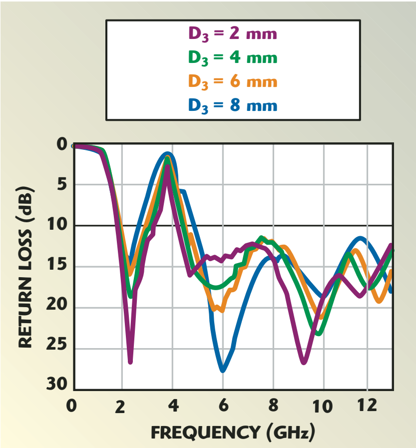
Different Values of D_1

Figure 3 shows the measured return loss for different length D_1. The other parameters are fixed: $W_1 = 32$ mm, $H_1 = 28$ mm, $H = 1$ mm, $G = 120$ mm, $S_1 = S_2 = 2$ mm, $D_2 = 8$ mm and $D_3 = 4$ mm. As D_1 increases, the rejected band moves to a lower frequency. It also shows that the bandwidth of the rejected band is not sensitive to D_1.

Different Values of D_2

Figure 4 shows the measured return loss with different length D_2. The

other parameters include: W_1 = 32 mm, H_1 = 28 mm, H = 1 mm, G = 120 mm, S_1 = S_2 = 2 mm, D_1 = 10 mm and D_3 = 4 mm. As D_2 increases, the rejected band also moves to a lower frequency. It also shows that the bandwidth of the rejected band is not sensitive to D_2. The length of $(D_1 + D_2) - (S_1 + S_2)$ is approximately equal to the overall length of the slit. It is expected that the rejected band of the proposed design will move to a lower frequency as D_1 or D_2 are increased.



▲ *Fig. 5 Measured return loss for different lengths of D_3.*

Different Values of D_3

Figure 5 shows the measured return loss with different length D_3, the other parameters being: W_1 = 32 mm, H_1 = 28 mm, H = 1 mm, G = 120 mm, S_1 = S_2 = 2 mm, D_1 = 10 mm and D_2 = 8 mm. As D_3 increases, the center frequency of the rejected band is slightly affected. However, the bandwidth of the proposed antenna is strongly affected by the length of D_3. When D_3 increases, the L-shaped slit is moved toward the antenna feed and the bandwidth of the rejected band is monotonically increased. ***Table 1*** is a summary of the antenna characteristics for different values of D_3. It is also observed that the bandwidth of the rejected band varies from 24 to 56 percent, which is suitable for the proposed application.

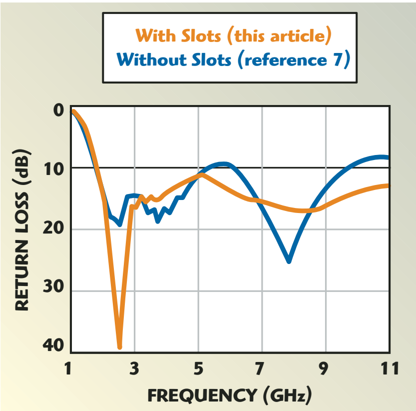
A DESIGN FOR UWB APPLICATIONS

An antenna design for a UWB system has been implemented. The measured return loss of the proposed antenna with dimensions H_1 = 28 mm, W_1 = 32 mm, H = 1 mm, G = 120 mm, S_1 = S_2 = 2 mm, D_1 = 6 mm, D_2 = 4 mm and D_3 = 8 mm is plotted in ***Figure 6*** and is compared to a cross semi-elliptic monopole antenna without slots of similar dimensions.[7] The rejected band of this proposed antenna is from 5.15 to 6.04 GHz, which fits the requirement of the DS-UWB proposal.[8] In other words, this design succeeds in suppressing the interference between the UWB and WLAN systems. The measured results for the band-rejected antenna proposed show operating bandwidths of 1.85 to 5.29 GHz and 6.3 to 9.8 GHz for a return loss greater than 10

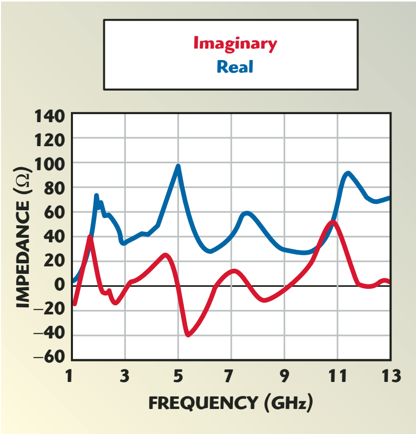
TABLE I

SUMMARY OF THE ANTENNA CHARACTERISTICS FOR DIFFERENT VALUES OF D3

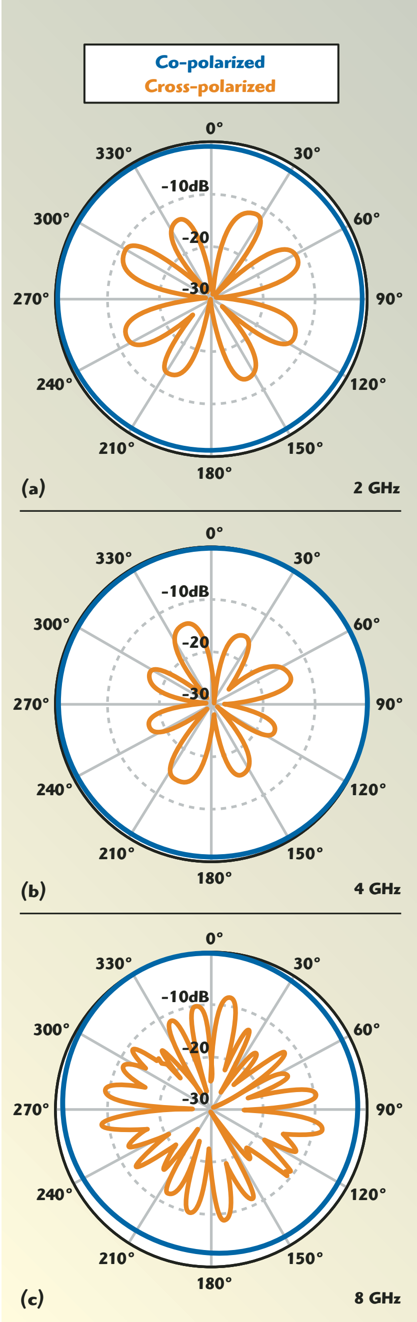
D3 (mm)	Center Frequency of Rejected Band (f_c) (GHz)	Return Loss at f_c (dB)	Frequency Range of Rejected Band (GHz)	Bandwidth of Rejected Band (%)
2	3.841	2.812	3.33~4.25	24
4	3.841	1.902	3.13~4.49	35
6	3.841	1.335	2.81~4.62	47
8	3.9055	1.110	2.74~4.94	56



▲ *Fig. 6 Measured return loss of cross semi-elliptic disc monopole antennas for UWB application.*



▲ *Fig. 7 Measured impedance of the proposed antenna.*



▲ *Fig. 8 Measured radiation patterns in the x-y plane of the proposed antenna.*

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DAT-15575-P ▲	Parallel	75	DC-2000	15.5	0.5	5	3.55
DAT-15575-S ▲	Serial	75	DC-2000	15.5	0.5	5	3.55
DAT-31-P ▲	Parallel	50	DC-2400	31.0	1.0	5	3.55
DAT-31-S ▲	Serial	50	DC-2400	31.0	1.0	5	3.55
DAT-3175-P ▲	Parallel	75	DC-2000	31.0	1.0	5	3.55
DAT-3175-S ▲	Serial	75	DC-2000	31.0	1.0	5	3.55
DAT-31R5-P ▲	Parallel	50	DC-2400	31.5	0.5	6	3.80
DAT-31R5-S ▲	Serial	50	DC-2400	31.5	0.5	6	3.80
DAT-31575-P ▲	Parallel	75	DC-2000	31.5	0.5	6	3.80
DAT-31575-S ▲	Serial	75	DC-2000	31.5	0.5	6	3.80

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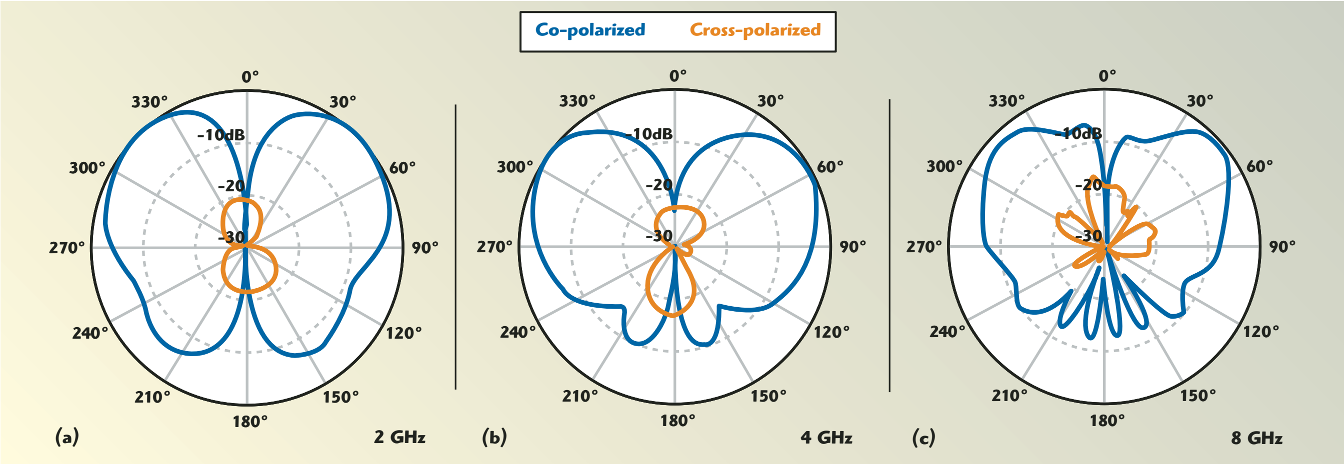
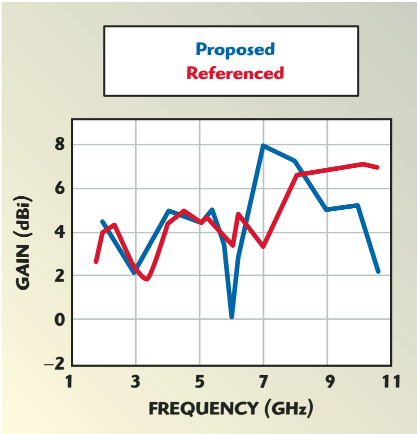


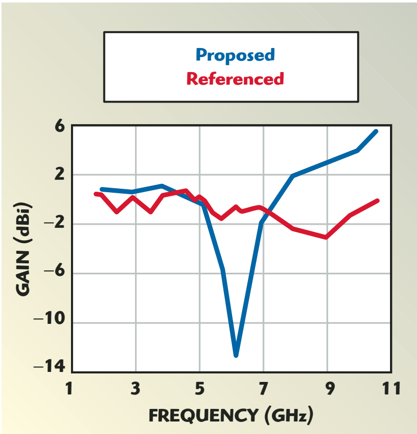
▲ *Fig. 9 Measured radiation patterns in the y-z plane of the proposed antenna.*

dB. ***Figure 7*** shows the real and imaginary impedances of the proposed antenna. It is found that the real impedance of the proposed antenna is dramatically increasing within the rejected frequency band, while the imaginary impedance is rapidly changing, leading to the band-rejected characteristics of the antenna.

Figure 8 shows the measured radiation patterns of the proposed antenna in the x-y plane at f = 2, 4 and 8 GHz. The x-y plane radiation patterns are almost omni-directional. ***Figure 9*** shows the radiation pattern in the y-z plane. The measured patterns of the proposed antenna are dipole-like radiation, which makes the proposed antenna suitable in practical UWB applications. The measured x-y plane peak antenna gain for the referenced antenna[7] and the proposed antenna are shown in ***Figure 10*** over the impedance bandwidth. It is obvious that the proposed antenna with four L-shaped slits significantly affects the x-y plane peak gain within the rejected bandwidth. The measured y-z plane peak antenna gains for the referenced antenna and the proposed an-



▲ *Fig. 10 Measured x-y plane peak antenna gain for the proposed antenna and the antenna of reference 7.*



▲ *Fig. 11 Measured y-z plane peak antenna gain for the proposed antenna and the antenna of reference 7.*

tenna over the impedance bandwidth are shown in ***Figure 11***. It is obvious that the proposed antenna with four L-shaped slits significantly affects the x-y and y-z plane peak gains over the band-rejected bandwidth. Compared with the gain of the referenced antenna, the proposed antenna shows a maximum gain drop of approximately 12.2 dBi at 6.2 GHz in the y-z plane and a maximum gain drop of approximately 3.2 dBi at 6.0 GHz in the x-y plane. Therefore, the gain drop over the rejected band of the proposed antenna is significantly improved, compared to the referenced antenna with four narrow slits.[7]

CONCLUSION

A band-rejected cross semi-elliptic monopole antenna with four L-shaped slits has been implemented and investigated. The experimental results show that the impedance bandwidth obtained for this antenna design fits the requirements of wireless applications. The dipole-like radiation patterns over the operating bandwidth are also shown. In addition, the proposed antenna shows a good gain drop within the rejected band, compared to a corresponding cross semi-elliptic monopole antenna with four narrow slits.[7] The proposed design of this antenna is suitable for practical wireless applications. ■

ACKNOWLEDGMENT

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A FEED-FORWARD AMPLIFIER USING AN EQUAL GROUP-DELAY SIGNAL CANCELLATION TECHNIQUE

In this article, new signal cancellers that can match the out-of-phase and group delay of two signal paths simultaneously are proposed. The simultaneous matching of the out-of-phase and group-delay time between two paths can permit broadband signal cancellation. A feed-forward linear power amplifier that uses the proposed signal cancellers was fabricated for the IMT-2000 base station transmitting band. The main signal cancellation (first) loop of the fabricated feed-forward amplifier cancels the input signal by more than 26.3 dB and the intermodulation distortion (IMD) signal cancellation (second) loop cancels the IMD signal by more than 15.2 dB over a 200 MHz bandwidth. In the two-tone signals amplification process, the C/I ratio of the amplifier was improved by 21.2 dB, where the two tones were 2115 and 2165 MHz (Δf=50 MHz), respectively.

Modern wireless communication systems utilize digital modulation techniques employing linear complex coding schemes to maximize the channel throughput available capability. Also, a broader channel bandwidth is used for more data transmission than before. In addition, as various communication services, such as cellular phone (IS-95), personal communication service (PCS), IMT-2000 and mobile Internet are provided, the service frequency bandwidth is also broadened. These linear modulation schemes increase the peak-to-average ratio of the RF signal and the envelope variation of the signal is changed seriously.

A power amplifier is usually operated in the saturation region for maximum efficiency and high output power. As the power amplifier operates close to saturation, its linearity degradation becomes significant, due to the nonlinear characteristic of the power amplifier. Therefore, to the power amplifier designer, high linearity and high efficiency are critical issues. Hence, a compromise between power efficiency and linearity must be considered, otherwise a linearization technique to overcome the nonlinearity of the power amplifier is the only solution.

Various linearization methods, such as feed-forward, feedback, predistortion, LINC (linear amplification with nonlinear components), CALLUM (combined analog locked-

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loop universal modulator) and EER (envelope elimination and restoration) have been reported.[1,2] The analog predistortion method is conceptually the simplest form of linearization for an RF power amplifier, but its intermodulation reducing effect is not as good as for the feed-forward method. Digital predistortion shows good linearization results, but has a limited linearization frequency bandwidth because of the memory effect.[3–6] Among the numerous amplifier linearization techniques, feed-forward linearization has been extensively used in base station amplifiers, because of its intrinsic advantages of providing high linearity and a broadband linearizing bandwidth.[1–3] Although the feed-forward method can linearize over a broader band than any other linearizing methods, the bandwidth, for more than 20 dB reduction of the IMD components, is limited in practice. Previously, several broadband feed-forward applications, having a delay line phase equalizer or a multi-stage hybrid, have been presented.[7,8] However, the phase equalizer has difficulty in matching the phase characteristics of the power amplifier, because the amplifier consists of several transistor stages and its phase characteristics change according to the operating conditions and case-by-case differences. The multi-stage 3 dB hybrid method uses only its broadband characteristics. The previous approaches focus on the amplitude and out-of-phase matching between the two paths of the feed-forward loop, but ignore the group-delay matching. In this article, new signal cancellers that match the broadband out-of-phase and group-delay characteristic simultaneously between the two paths of the feed-forward loop are proposed. The proposed cancellers provide broadband signal cancellation in the feed-forward loop.

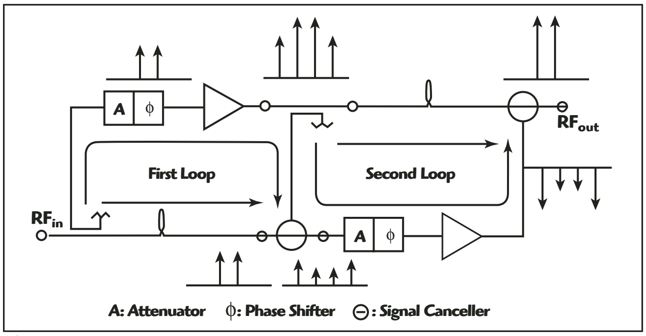


Fig. 1 Block diagram of a feed-forward amplifier.

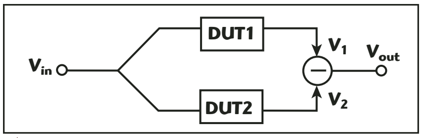


Fig. 2 Equivalent loop of the feed-forward amplifier.

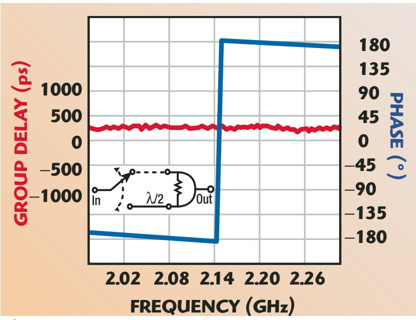


Fig. 3 Phase and group delay transmission characteristics of a Wilkinson canceller.

THEORY OF OPERATION OF A LINEARIZER

Analysis of a Feed-forward Equivalent Loop

Basically, a feed-forward amplifier consists of two signal cancellation loops that have the same operating principle and the same frequency components are cancelled in each loop. ***Figure 1*** shows the block diagram of a feed-forward amplifier, where the principle of operation is well illustrated for a two-tone spectrum. ***Figure 2*** shows an equivalent loop of the feed-forward amplifier for amplitude analysis, and phase and group-delay matching. Assuming that the signal in each path of the equivalent loop is sinusoidal, then the signal in the two paths can be written as

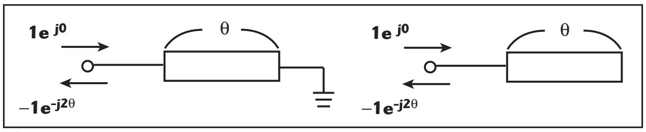


Fig. 4 Comparison of a reflected signal for transmission lines terminated in a short and open circuit.

$$V_1 = V_{1m}\cos\left(\omega_0 t - \phi\right) \qquad (1)$$

$$V_2 = V_{2m}\cos\left(\omega_0 t - \phi\right) \qquad (2)$$

where

$V_{1m} = V_{2m} + \Delta V,\ \theta = \phi + \pi + \Delta\phi$

If there are amplitude, phase and delay mismatchings between the two paths, then the cancellation performance (CP) can be written as[9]

$$CP = 10\log\left[1 + \alpha^2 - 2\alpha\cos\left\{2\pi\left(\frac{\lambda_{err}}{\lambda_0}\right)\left(1 - \frac{f}{f_0}\right) \pm \Delta\phi\right\}\right] \qquad (3)$$

where f_0 and λ_0 are the center frequency and wavelength. α, $\Delta\phi$ and λ_{err} are the amplitude, phase and group-delay mismatching parameter, respectively. The amplitude and the phase matchings are important for single frequency component cancellation, but the group-delay time matching is also an important parameter for broadband signal cancellation. ***Figure 3*** is a good example of the importance of group-delay matching in the feed-forward loop, where the characteristics of a Wilkinson canceller, which is one of the usual signal cancellers, are shown. The transmission phase and group-delay characteristics of a Wilkinson canceller, with one input port connected to a $\lambda_0/2$ transmission line, were measured. If the signals in the two paths have equal amplitude, linear phase characteristics and slight group-delay mismatching due to the $\lambda_0/2$ transmission line, then a perfect signal cancellation would be obtained around the center frequency. However, a signal at a ±100 MHz frequency offset would be partially cancelled due to its group-delay time mismatching. As a result, group-delay matching is shown to be important on broadband signal cancellation, in addition to the amplitude and phase matching.

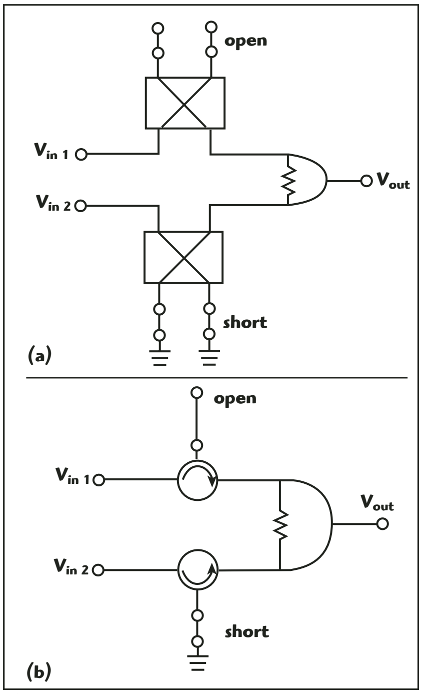
Design of an Equal Group-delay Signal Canceller

Figure 4 shows transmission lines terminated with short and open circuits. If the transmission lines have the same electrical length, the reflection signals are $-1e^{-j2\theta}$ and $1e^{-j2\theta}$, respectively. The reflection signals are out-of-phase, but their group-delay time is the same. Even though the input signal condition and the length of trans-

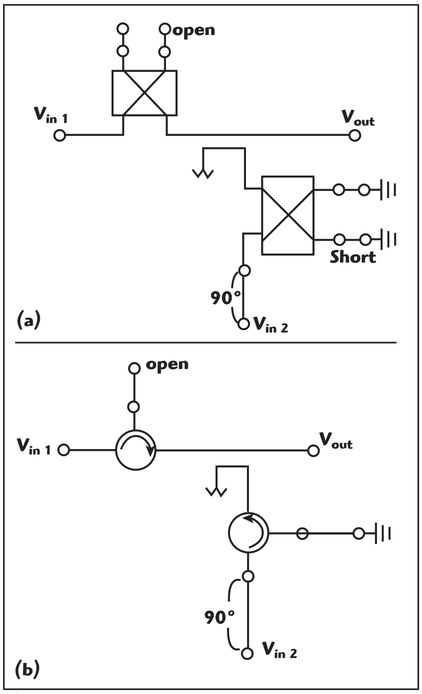
mission line are changed, these properties are not. ***Figure 5*** shows the block diagrams of the proposed first loop signal cancellers of the feed-forward amplifier. The two input signals of the hybrid-based circuit are fed to a 3 dB hybrid for which the coupling and the through ports are terminated with open and short circuits, respectively. The two output signals of the 3 dB hybrids are out-of-phase and fed into an in-phase combiner. Since the two input signals in the final output port experience the same group-delay time and are out-of-phase, a perfect signal cancellation is obtained. The 3 dB hybrid is used to obtain a good reflection characteristic. The 3 dB hybrid could be replaced with a circulator. However, the frequency dependence of a circulator is more severe than for a 3 dB hybrid. So the use of hybrids is preferable in the first loop signal canceller. ***Figure 6*** shows the block diagrams of the second loop signal canceller of the feed-forward amplifier. The operating principle of the second loop canceller is almost the same except for the 90° phase compensation of the loose coupling hybrid.

MEASURED RESULTS

To show the validity of a feed-forward amplifier adopting the proposed signal cancellers, several circuits such as a main amplifier, an error amplifier, variable attenuators and variable phase shifters as well as the proposed first and second cancellers, using 3 dB hybrids, were fabricated. For comparison, a Wilkinson combiner and a 10 dB hybrid were also fabricated as conventional signal cancellers, where the operating frequency was 2.14 ±0.1 GHz. The feed-forward amplifiers used the same circuits except for the cancellers, because the cancellation results of the feed-forward amplifier depended on the electrical characteristics of the sub-circuits. The fabricated main and error amplifiers consisted of four transistor stages. The measured gain, maximum return loss and 1 dB compression point (P1dB) were 44.7 ±0.3 dB, –14 dB and 28.7 dBm, respectively. The variable attenuator and the variable phase shifter were of the reflection type for good reflection characteristics. The maximum attenuation and phase shifting range were 15 dB and 120°, respectively. ***Figure 7*** shows the first loop signal cancellation characteristics, using the conventional Wilkinson and the proposed signal cancellers. The input signal was cancelled more than 16.4 dB within 2.14 ±0.1 GHz with the conventional Wilkinson canceller. However, the proposed canceller can-



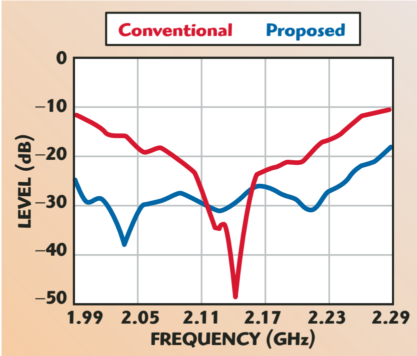
▲ *Fig. 5 Proposed first loop signal cancellers (a) using hybrid couplers and (b) using circulators.*



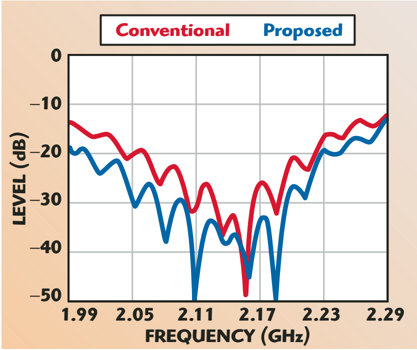
▲ *Fig. 6 Proposed second loop signal cancellers (a) using hybrid couplers and (b) using circulators.*

celled the signal more than 26.3 dB within the same frequency range. The frequency bandwidth where the signal was cancelled by more than 20 dB was broader than 300 MHz.

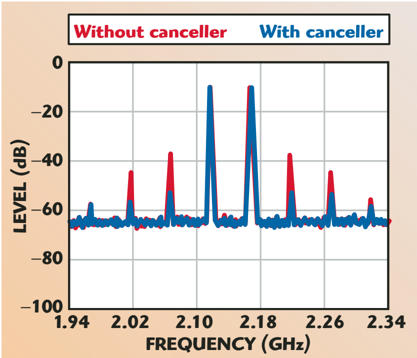
Figure 8 shows the second loop signal cancellation characteristic using the conventional canceller and the proposed canceller. The input signal was cancelled by more than 11.7 dB within 2.14 ±0.1 GHz with the conventional canceller. However, the proposed canceller cancelled by more than 15.2 dB within the same frequency range. The frequency bandwidth that the signal was cancelled more than 20 dB was improved from 94 to 173 MHz. With a two-tone signal amplification process, the improvements in the carrier-to-intermodulation (C/I) ratio were also measured, where the two-tone signals were 2115 and 2165 MHz, respectively. Before the error path of the second loop was connect-



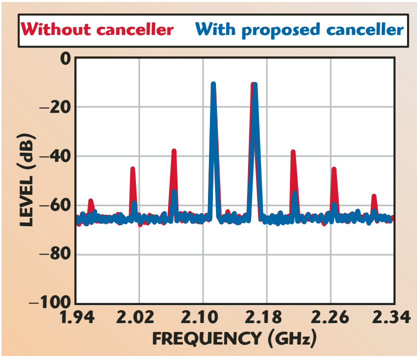
▲ *Fig. 7 Signal cancellation characteristics of the first loop using a conventional and the proposed cancellers.*



▲ *Fig. 8 Signal cancellation characteristics of the second loop using a conventional and the proposed cancellers.*



▲ *Fig. 9 Output characteristics of the feed-forward amplifier with and without conventional cancellers.*



▲ *Fig. 10 Output characteristics of the feed-forward amplifier with and without proposed cancellers.*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ed, the C/I ratio and the output power level at the feed-forward amplifier output port were just 26.84 dBc and 17.5 dBm/tone, respectively. When the amplifier was linearized with the conventional cancellers, the C/I ratio was improved to 42.63 dBc. ***Figure 9*** shows the output characteristics of the feed-forward amplifier with and without the conventional cancellers. The improvement of the fifth C/I was not good, whereas that of the third C/I was fairly good. That was due to the out-of-phase and group-delay mismatching of the cancellers in the feed-forward loop. When the amplifier was linearized with the proposed cancellers, the C/I ratio was improved to 48.03 dBc. ***Figure 10*** shows the output characteristics of the feed-forward amplifier with and without the proposed cancellers. The third C/I was improved as well as the fifth C/I. The comparison of the C/I measurements, between the conventional and the proposed feed-forward amplifier, shows that the proposed cancellers improve C/I over a broader band.

CONCLUSION

In this article, new signal cancellers are proposed that match simultaneously the phase and group-delay properties of the feed-forward loops. Conceptually, a feed-forward amplifier that adopts the proposed cancellers can cancel carrier signals in the first loop and IMD signals in the second loop perfectly over a broad band. IMT-2000, mobile Internet and wireless LAN using OFDM have a broader service frequency bandwidth than previous other communication services. A feed-forward amplifier, using conventional cancellers, is limited in linear frequency bandwidth, so that it cannot operate over the necessary frequency band. However, the proposed feed-forward amplifier can be linearized over the whole frequency band without a partition of the service band. The proposed feed-forward amplifier may be advantageous to communication service providers and amplifier manufacturers, because of better operating convenience and good manufacturing yield. ■

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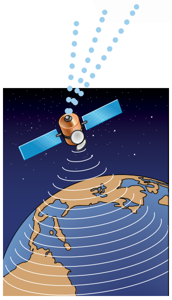

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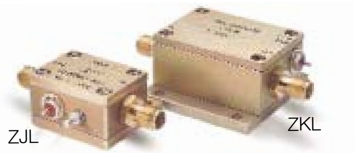
ZJL-7G	20-7000	10.0	±1.0	8.0	5.0	24.0	50	99.95
ZJL-4G	20-4000	12.4	±0.25	13.5	5.5	30.5	75	129.95
ZJL-6G	20-6000	13.0	±1.6	9.0	4.5	24.0	50	114.95
ZJL-4HG	20-4000	17.0	±1.5	15.0	4.5	30.5	75	129.95
ZJL-3G	20-3000	19.0	±2.2	8.0	3.8	22.0	45	114.95
ZKL-2R7	10-2700	24.0	±0.7	13.0	5.0	30.0	120	149.95
ZKL-2R5	10-2500	30.0	±1.5	15.0	5.0	31.0	120	149.95
ZKL-2	10-2000	33.5	±1.0	15.0	4.0	31.0	120	149.95
ZKL-1R5	10-1500	40.0	±1.2	15.0	3.0	31.0	115	149.95

NOTES:
1. Typical at 1 dB compression.
2. ZKL dynamic range specified at 1 GHz.
3. All units at 12V DC.



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CMOS Oscillator Design Considerations

The oscillator is a critical part of modern wireless communication systems. It is the local oscillator that is used to up-convert the baseband signal to the desired RF frequency in the transmitter. Vice versa, the local oscillator is used to down-convert the desired signal in the receiver. In the past, the oscillator has been mostly implemented with discrete transistors and stands as an individual module. With advances in CMOS technology, complete CMOS transceivers have become very common. Integrated CMOS oscillators are replacing discrete oscillators in more and more applications.

This article is intended to present four commonly used CMOS oscillator topologies.

There are many design considerations involved. The phase noise of the oscillator directly impacts the system's overall performance. For example, the phase noise of the VCO affects the cell phone receiver adjacent channel rejection performance. Its current consumption is a major part of the overall receiver power budget as in a low power GPS receiver. Since an inductor is used in the oscillator design, the real estate of the oscillator is a high percentage of the overall IC. There are many design topologies available to the designers. There is no single design that will fit all the requirements. It is the designer's job to determine the most suitable topology based on the applications and requirements. This article is intended to present four commonly used CMOS oscillator topologies. Their theory of operations is presented and their pros and cons are discussed in detail.

The first topology presented is an inductorless, generic, three-stage ring oscillator. The ring oscillator typically has an odd number of stages to prevent latch up. Each stage provides an equal amount of the gain and phase shift needed. Its schematic is shown in ***Figure 1***. It is a much simpler circuit than it looks. This circuit contains three identical gain stages. M1 to M6 forms the first gain stage. To further simplify the analysis, only the left half of stage 1 is examined. M1 is the NMOS that provides the gain. M4 is essentially a diode-connected PMOS load. M3 is used as a trick to enhance the gain. The gain of the diode-connected load amplifier depends on the geometry of both NMOS and PMOS. The gain equation is

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$$\text{gain} = -\sqrt{\frac{\mu_n \left(\frac{W}{L}\right)_N}{\mu_p \left(\frac{W}{L}\right)_P}} \qquad (1)$$

where

W/L = channel width over channel length ratio

In order to get a higher gain, W/L for the PMOS device needs to be small. However, this will result in a higher overdrive voltage for the PMOS device since the bias current is fixed. Thus, it will reduce the voltage swing at the drain of the PMOS and NMOS transistors. The trick is to bias M3 to "steal" part of the bias current that has to flow in the PMOS. This way, a compromise is reached between voltage gain and voltage swing range. M2, M5 and M6 provide the other half of the differential gain stage. The first gain stage is repeated three times to complete the overall ring oscillator. The outputs of each stage are taken at the drains and the inputs are located at the gates. The positive side of the output drives the positive input of the next stage. The exception happens at the last stage where the positive output drives the negative input. The reason is that each gain stage provides a 60° phase shift at the frequency of operation. The three stages provide a 180° phase shift. The remainder of the phase shift comes from the output inversion. The frequency tuning is done by controlling the bias current. The most attractive feature of this topology is that no inductor is used. It saves a large amount of real estate. The design is also very simple to implement since identical gain stages are used. No varactor design is needed since the frequency control is accomplished by varying the bias current. The best feature of this topology is also the root of its problem. Without an LC filter bank, the phase noise performance is much worse.

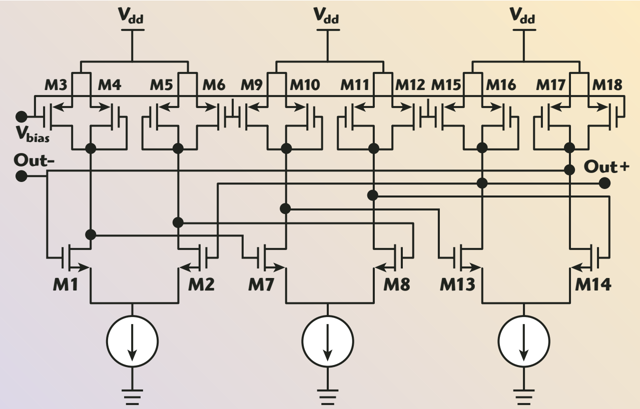

Fig. 1 The CMOS ring oscillator.

To improve the phase noise performance, an oscillator with an LC tank is typically preferred. Its basic form is presented in ***Figure 2***. The basic idea is based on negative resistance theory. An oscillator can be reduced to a simple parallel RLC (resistor, inductor and capacitor) circuit. In an ideal oscillator, the parallel resistance should be infinite. The energy is transferred back and forth between the inductor and the capacitor. A positive resistance means that some of the energy will be taken away by the resistor and dissipated as heat. If the positive resistor takes energy, then a negative resistor must provide the energy to sustain the oscillation. This is the fundamental idea of this topology. M1 and M2 form the VCO core. By cross coupling M1 and M2, the positive feedback provides a negative impedance looking back into the drain of M1 and M2. The negative impedance is given by

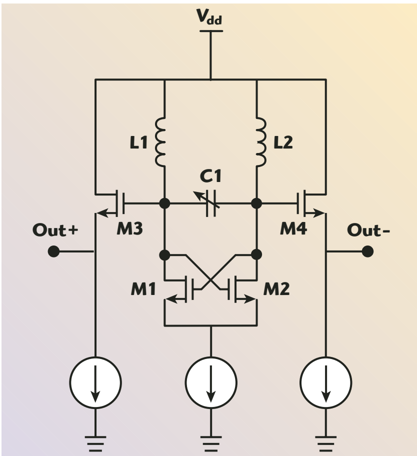

Fig. 2 NMOS-only cross-coupled oscillator.

$$Z(\text{neg}) = -\frac{2}{g_m} \qquad (2)$$

where

g_m = transconductance of the NMOS

Here, the varactor tuning diode is represented by a variable capacitor. L1 and L2 each form half of the inductance for the LC tank. M3 and M4 are the source followers. They are the output buffer to help lower the output impedance in order to drive the mixer efficiently. This topology is easy to understand and relatively easy to implement. It offers good phase noise and good tuning range. It has been a very popular topology for the oscillator designer. There is still room for improvement in the area of power efficiency. This will lead to the third oscillator topology.

The third oscillator topology, shown in ***Figure 3***, is typically labeled a complementary cross-coupled oscillator. It gets its name because both NMOS and PMOS devices are used to obtain the negative resistance. M1, M2, M5 and M6 are the active elements contributing to oscillation. M3 and M4 are the output buffers. During half the cycle, M1 and M6 are on while M2 and M5 are off. The full bias current flows through the RLC network. Vice versa, during the other half of the cycle, M2 and M5 are on while M1 and M6 are off. This is the major difference between the cross-coupled oscillator and the NMOS-only cross-coupled oscillator. Note that the sum of L1 and L2 in the NMOS-only cross-coupled oscillator is equivalent to L1 in the complementary cross-coupled oscillator. In the NMOS-only design, during each half cycle of the oscillation, the bias current only flows through one half of the inductor. Because of this, the cross-coupled design has many advantages over the NMOS-only. First, the cross-coupled oscillator is twice as power efficient as the NMOS-only design. Second, the voltage swing in the cross-coupled oscillator is twice that of the NMOS-only oscillator, which improves the phase noise by 6 dB. Thus, the cross-coupled oscillator is becoming the oscillator of choice by more and more designers.

There are many design variations derived from the complementary cross-coupled oscillator topology. One topology is to eliminate the bias current source. Voltage bias at the gate of the active element is used instead. The bias current source is typically implemented with a current mirror. Without the NMOS for a current mirror, the design will gain extra overdrive voltage swing headroom. The downfall is a higher power consumption because of the higher voltage swing needed to drive the transistor. The other improvement includes adding an AC ground capacitor at the source of the FET. The idea is that the virtual ground at the source is not perfect. It has been reported to improve phase noise. The cross-coupled oscillator has its disadvantage as well. Because the PMOS performance is typically lower than the NMOS for the same geometry, the upper frequency range will be compromised compared to an NMOS-only topology. Since the transconductance of the PMOS is lower than the NMOS, proper scaling is required. Otherwise an asymmetrical waveform will result.

The topologies of the cross-coupled oscillators can be used as a building block for a more advanced oscillator. In most wireless devices using digital modulation/demodulation, both I and Q channels are required. Traditionally, an oscillator is designed and then an extra device is used to convert the oscillator output to an I/Q signal path. In many IC designs, an RC network is used to get I/Q. However, a one-stage RC network has a very limited frequency range. It is not suitable for today's wideband, multi-

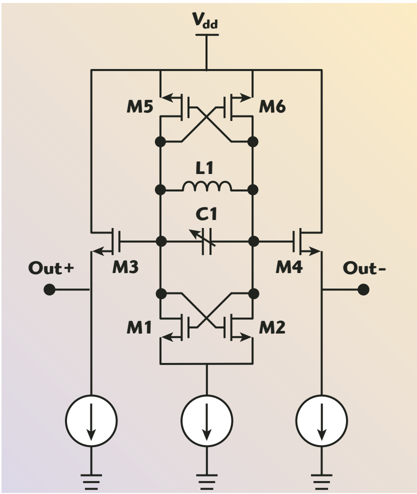

Fig. 3 Complementary cross-coupled oscillator.

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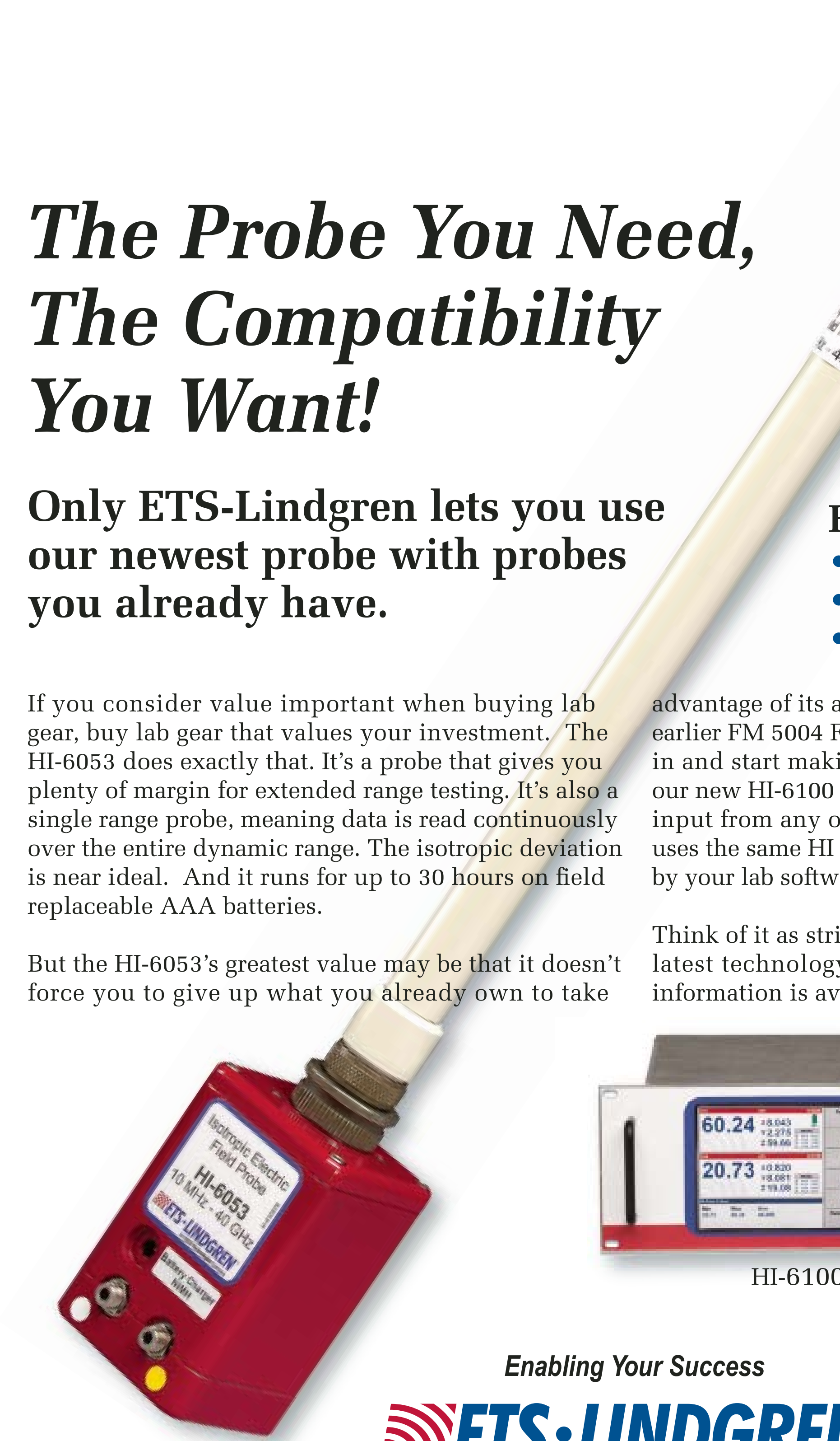

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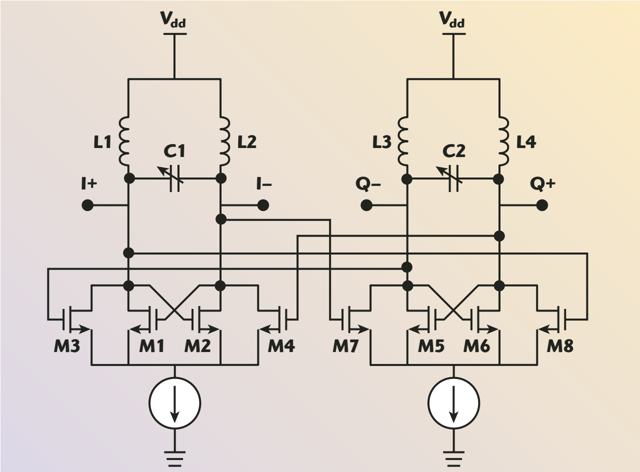

Fig. 4 A quadrature VCO.

ple-band, multiple-mode, highly integrated transceivers. To improve the frequency range, multi-stage RC polyphase filters are used. But the issue is high insertion loss through the RC network; hence, the power efficiency suffers. A better design is to use a quadrature VCO (QVCO), as shown in ***Figure 4***. The QVCO is based on the idea of sympathetic oscillation. With proper coupling, a pair of VCOs can oscillate in harmony. An NMOS-only oscillator is used as the basic building block. M1 to M4 along with the LC tank form the first oscillator. M5 to M8 complete the second oscillator. M1, M2, M5 and M6 are the negative resistance generating active elements. M3, M4, M7 and M8 make up the output buffers. The circuit design itself is straightforward once the individual VCO design is under control. Compared with the polyphase RC network-based I/Q generation, QVCO is far more efficient in power and space. One area that needs to be watched is bimodal oscillation. Basically the QVCO will oscillate either with 90° phase shift or –90° phase shift. Both phase shifts satisfy the oscillation requirement. Bimodal oscillation is highly undesirable. It can be resolved by introducing a proper phase shift in the buffer driver circuit. By using a cascade topology in place of the M3, M4, M7 and M8, bimodal oscillation is eliminated.[1]

CONCLUSION

This article has presented commonly used CMOS oscillator topologies. Each topology has its own advantages and disadvantages. There are many tradeoffs involved as in most RF designs. For applications with tight space requirements and relaxed phase noise, the ring oscillator is a good choice. For best power efficiency, the cross-coupled oscillator deserves strong consideration. For simplicity and higher frequency operation, the NMOS-only oscillator is still a good candidate. All the basic oscillator topologies can be reused in a more complex design like the QVCO. There are still many practical design considerations involved in inductor and varactor designs. With so many design choices, oscillator designers need to choose the right topology based on the application at hand. ■

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A Practical Method for Determination of HBT Thermal Resistance and Its Power Dependence

A practical and reliable method for the determination of thermal resistance and its power dependence is presented. This method requires only forward Gummel data at different ambient temperatures and at different collector-emitter bias voltages. The determined thermal resistance was successfully used to calculate the junction temperature in a DC model of a 2 × 25 μm² GaInP/GaAs HBT device.

Heterojunction bipolar transistors (HBT) have demonstrated high power output densities at microwave frequencies and are increasingly utilized in the design of RF circuits such as power amplifiers, oscillators and mixers.[1] Thus, an accurate large-signal model for HBT devices is of great importance in designing such circuits, especially when the transistor is operated in nonlinear regions where self-heating effects become significant. Although the temperature sensitivity of transistor parameters is significant for all types of power transistors, it is particularly important for the HBT, with its relatively poor thermal conductivity. It is well known that the saturation currents and ideality factors of model diodes change with ambient temperature. This change has been fitted to exponential and polynomial functions in HBT models.[2] However, if it is assumed that the saturation currents and ideality factors remain fixed at their ambient temperature values, their associated temperature dependence can be attributed to the increase of the base-emitter voltage by an incremental thermal voltage V_{TH}.[3] This is illustrated as follows:

$$V_{be} = V_{be0} + V_{TH} \tag{1}$$

$$V_{TH} = \left|\frac{\partial V_{be}}{\partial T}\right| \Delta T \tag{2}$$

$$\Delta T = T_j - T_0 = R_{th} P_{dsp} \tag{3}$$

where

V_{be0} = base-emitter voltage at ambient temperature T_0
P_{dsp} = dissipated power in the device
R_{th} = thermal resistance

DETERMINATION OF THERMAL RESISTANCE

The proposed method of determining thermal resistance uses forward Gummel mea-

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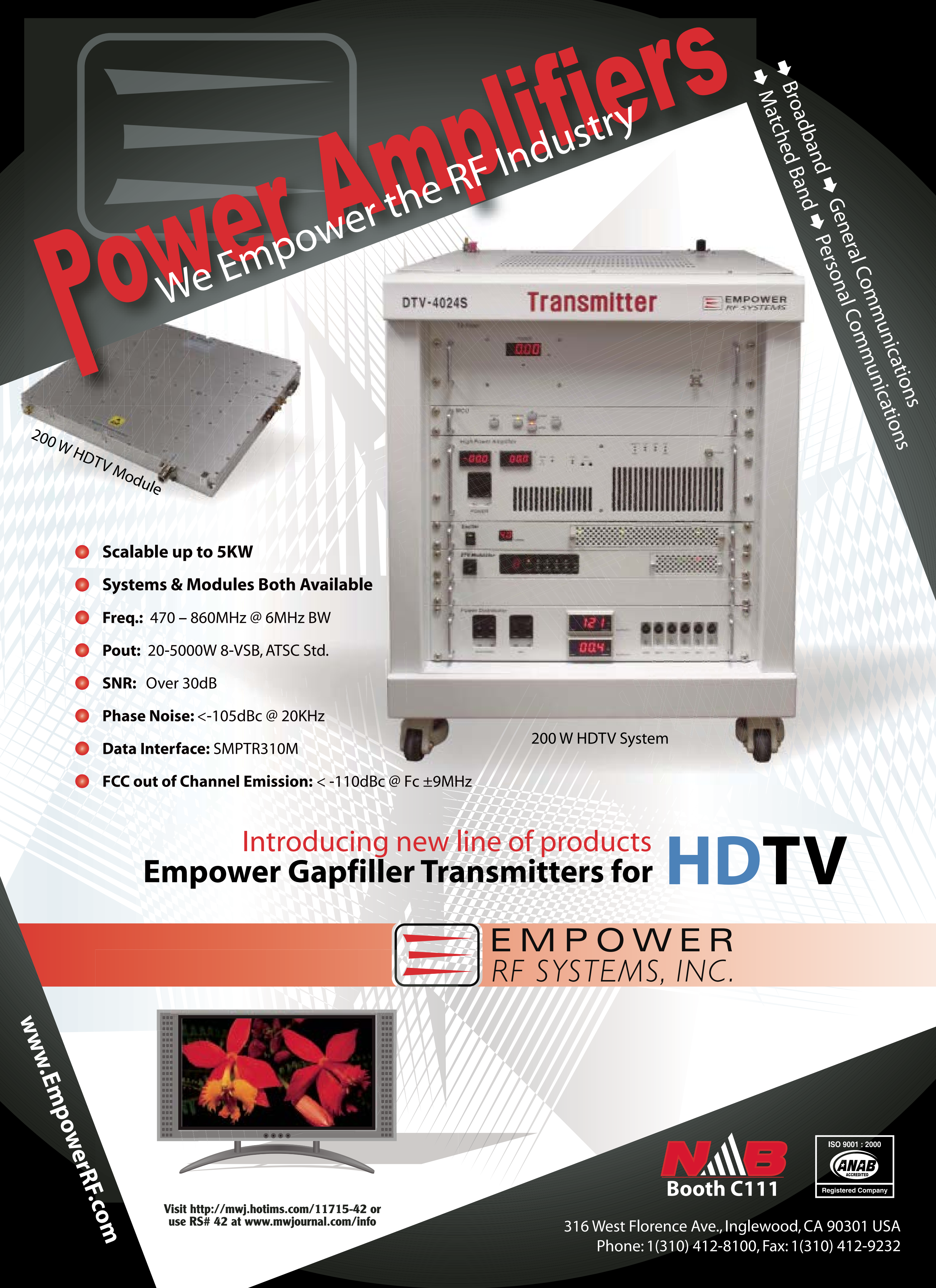
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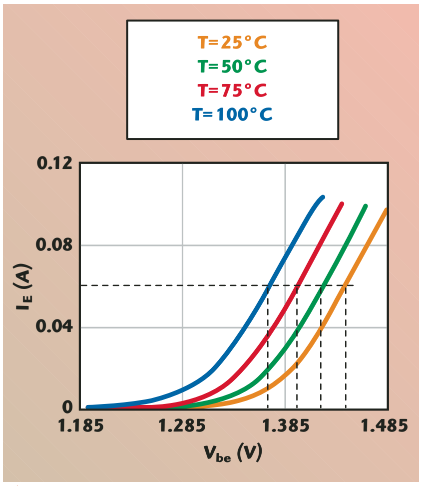
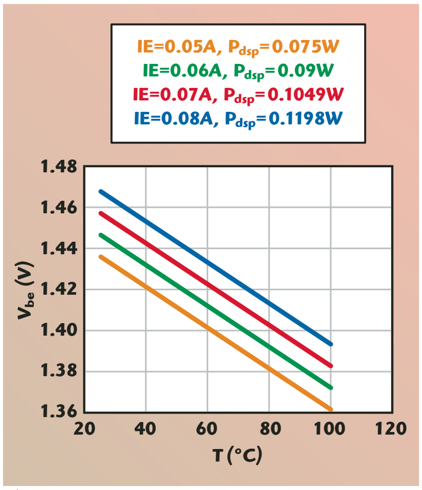
surements for different ambient temperatures and for different collector-emitter bias voltages V_{ce}. This method was applied to an on-wafer 2 × 25 μm² GaInP/GaAs HBT in a common-emitter configuration. The DC measurements were accomplished using a Cascade probe station, monitored by a program developed using HP-VEE software. A thermal chuck was used to set the ambient temperature of the device. MATLAB software was used for programming the extraction of the thermal resistance.

As proven by Zhang et al.,[4] for a constant emitter current I_E, the base-emitter voltage V_{be} varies linearly with the junction temperature T_j. Thus, around an arbitrary temperature $T_1(T_1 \geq T_0)$, the voltage V_{be} at temperature T_j can be written as



▲ *Fig. 1 Measured forward Gummel I_{EVS} V_{be} characteristics at different ambient temperatures (V_{ce}=1.5 V).*



▲ *Fig. 2 Base-emitter voltage V_{be} versus ambient temperature for different emitter currents I_E.*

$$V_{be}\left(T_j\right) = V_{be1} + \left.\frac{\Delta V_{be}}{\Delta T}\right|_{T_1}\left(T_j - T_1\right) \quad (4)$$

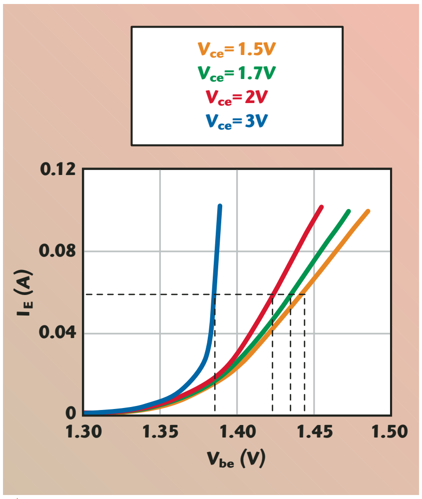
where

V_{be1} = base-emitter voltage at temperature T_1

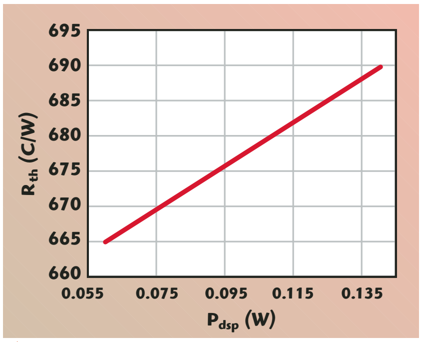
Knowing that $T_j = T_0 + R_{th}P_{dsp}$, Equation 4 becomes

$$V_{be}\left(T_0, P_{dsp}\right) = V_{be1} + \left.\frac{\Delta V_{be}}{\Delta T}\right|_{T_1}\left(T_0 - T_1\right) + \left.\frac{\Delta V_{be}}{\Delta T}\right|_{T_1} R_{th}P_{dsp} \quad (5)$$

Two sets of measurements are necessary to determine the thermal resistance R_{th}. The first set of measurements contains the Gummel data at a fixed collector-emitter voltage of 1.5 V and variable ambient temperature (see ***Figure 1***). The second set of measurements contains the Gummel data for a fixed ambient temperature (25°C) and a variable collector-emitter voltage. The extraction of the thermal resistance is illustrated in the following two steps:



▲ *Fig. 3 Measured forward Gummel characteristics I_E -V_{be} for different V_{ce} voltages (T=25°C).*



▲ *Fig. 4 Thermal resistance versus dissipated power (symbol: measured data, solid line: calculated using Eq. 9).*

Step 1

Considering the parameter P_1 as the slope of the linear variation of the voltage V_{be} versus the temperature T_1 while the dissipated power P_{dsp} is maintained constant, as shown in ***Figure 2***, one can write

$$P_1 = \left.\frac{\Delta V_{be}}{\Delta T}\right|_{T_1} \quad (6)$$

The dissipated power was calculated from: $P_{dsp} = I_cV_{ce}$ with $I_c \approx I_E$ since $I_c > 100I_b$ in the considered bias cases. The values of I_c and V_{ce} were determined at a 25°C ambient temperature in each case, for the considered emitter current I_E. In this first step, a set of values of the parameter

$$\frac{\partial V_{be}}{\partial T}$$

for different dissipated power is obtained.

Step 2

Considering the parameter P_2 as the slope of the linear variation of the base-emitter voltage V_{be} versus the dissipated power P_{dsp} (corresponding to a constant emitter current I_E) while maintaining the temperature T_1 constant, one can write

$$P_2 = \left.\frac{\Delta V_{be}}{\Delta T}\right|_{T_1} R_{th} \quad (7)$$

The dissipated power was calculated from $P_{dsp} = I_cV_{ce}$ with $I_c \approx I_E$. The values of I_c were determined at a 25°C ambient temperature in each case of the considered constant emitter current I_E (see ***Figure 3***). The collector-emitter voltage was fixed at 1.5 V. The values of the emitter current I_E were the same as those considered in the first step. In this second step, a set of values of parameter

$$\frac{\partial V_{be}}{\partial P_{P_{dsp}}}$$

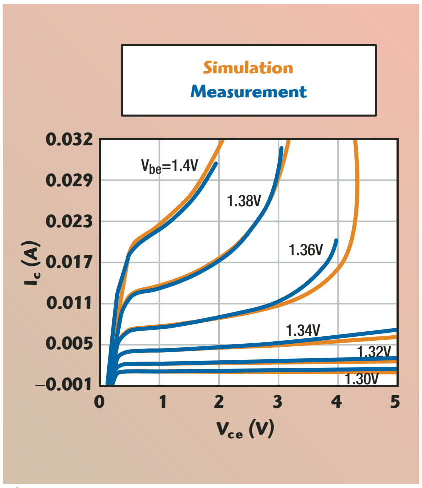
for different dissipated powers was obtained. The used values of the dissipated powers were the same as those determined in the first step.

Finally, using the values of parameters P_2 and P_1, the ratio P_2/P_1 was calculated, which allows for determi-

nation of the thermal resistance at each considered dissipated power P_{dsp} and emitter current I_E

$$R_{th} = \left.\frac{P_2}{P_1}\right|_{I_E} \qquad (8)$$

Experimental validation showed that the determined thermal resistance



▲ *Fig. 5 Measured and model-simulated I_c versus V_{ce} characteristics.*

varies linearly versus the dissipated power. As shown in ***Figure 4***, this variation is linear and can be calculated using the following derived formula

$$R_{th}\left(P_{dsp}\right) = 311.6P_{dsp} + 646.3 \qquad (9)$$

INCLUSION OF THERMAL EFFECT IN A HBT DC MODEL

The determined R_{th} was used to calculate dynamically the self-heating in a developed HBT DC model. A set of parameters for this model was determined, using methods reported previously.[5,6] The proposed HBT DC model was implemented in the commercial simulator ADS as a symbolically defined device (SDD). The implemented electro-thermal model has predicted accurately the DC characteristics of a 2 × 25 μm² InGaP/GaAs HBT device, as shown in ***Figure 5***.

CONCLUSION

A practical and detailed method for accurate determination of thermal resistance R_{th} and its power dependence was developed. This method used forward Gummel data at different ambient temperatures and at different collector-emitter bias voltages. The linearly power dependent thermal resistance was successfully used to calculate the junction temperature variation in a DC model of a 2 × 25 μm² GaInP/GaAs HBT device. ■

ACKNOWLEDGMENT

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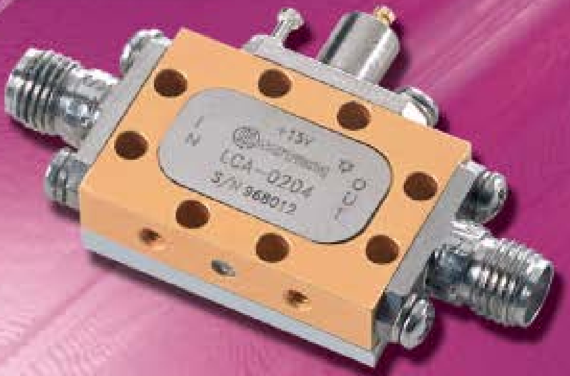

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LCA-0408	4 – 8	25	1.0	1.5	2:1	2:1	10	200
LCA-0812	8 – 12	25	1.0	1.8	2:1	2:1	10	200
LCA-1218	12 – 18	25	1.5	2.8	2:1	2:1	10	200
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DESIGN OF THREE-LINE MULTI-LAYER MICROSTRIP DIRECTIONAL COUPLERS AT HF FOR HIGH POWER APPLICATIONS

A practical method for designing three-line microstrip directional couplers at high frequency (HF) for high power applications is given for the first time using multi-layer dielectrics. The forward-coupling slope characteristic of the directional coupler is used to obtain a directional coupler in the HF range. A three-line microstrip directional coupler, using multi-layer dielectrics, is designed and simulated using electromagnetic (EM) simulation tools and then constructed and measured. The measured results are found to be very close to the simulated results.

It is common practice to use directional couplers in the HF range (3 to 30 MHz) for high power RF/microwave applications, such as magnetic resonance imaging (MRI), plasma generation for semiconductor processing equipment and laser drivers, in order to measure the transmitted and reflected powers accurately. Microstrip-type directional couplers have several advantages over lumped-element-type directional couplers, such as ease of manufacture, repeatability and low cost. However, the length of the microstrip lines is inversely proportional to the operational frequency. As the operational frequency decreases, the length of the microstrip lines increases. As a result, it is impractical to implement microstrip designs in the HF range using conventional techniques because of the length factor. Three-line microstrip directional couplers have been investigated by many authors at microwave ranges.[1–3] To this author's knowledge, however, there has not been a single publication on the design of microstrip directional couplers using multi-layer structures in the HF range.

In this article, the design of a three-line microstrip directional coupler for high power RF applications in the HF range using multi-layer dielectrics is reported for the first time. This is accomplished by designing the directional coupler at a frequency that is higher than the operational frequency and using its forward-coupling slope characteristic to obtain the final design at the operational HF frequency. The multi-layer dielectric structure that is implemented in this design improves the

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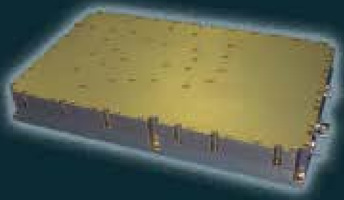

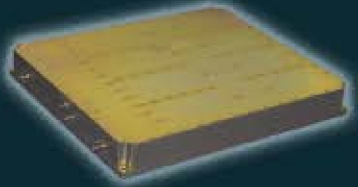

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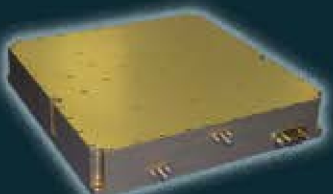
20 MHz - 1000 MHz
25 Watt RF Amplifier



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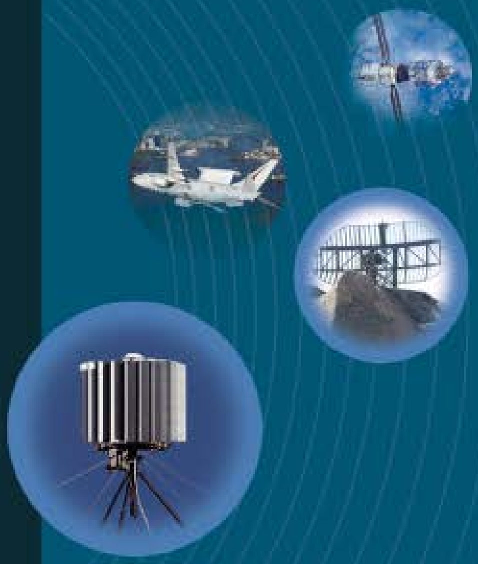

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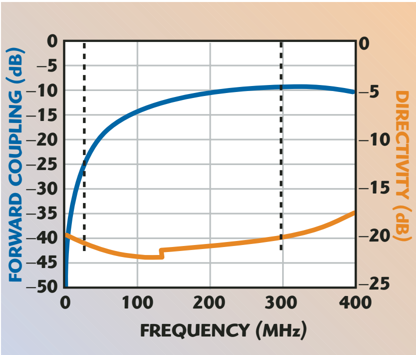
performance of the directional coupler by effectively increasing the minimum arcing distance between the coupled lines and the main line, which is necessary in high power applications. A three-line microstrip directional coupler is designed and then simulated using an EM simulation tool. The directional coupler is then constructed and measured. The simulation and the measured results are compared and found to be very close.

DIRECTIONAL COUPLER DESIGN

The operational frequency of the directional coupler is specified to be 27.12 MHz. This is a common operational frequency for plasma and MRI applications. The forward coupling of the directional coupler is specified to be –24 dB. Teflon is the specified substrate and is chosen because of its cost effectiveness. The physical length of the standard coupled lines would be impractically long to be realizable as mentioned in the introduction, when the operational frequency is in the HF range. For instance, a quarter-wavelength 50 Ω microstrip on a 100 mil-thick Teflon substrate at 27.12 MHz would be over 80 inches long. One way to overcome this problem is to design the directional coupler at a higher frequency and use its forward-coupling slope characteristic to have the desired coupling level at the operational frequency. This reduces the physical length of the directional coupler significantly and gives the desired coupling level at the operational frequency. For this reason, a three-line directional coupler at 300 MHz for a –10 dB forward-coupling level was designed using a method of moment (MoM)-based field solver. A two-layered Teflon dielectric structure was used. Each layer in the multi-layer structure is 60 mils thick. The EM simulation is performed initially to confirm the design and obtain the final physical parameters of the directional coupler. EM simulation results are then verified with the experimental results.



▲ *Fig. 1 Simulated forward coupling and directivity.*

▲ *Fig. 2 The constructed directional coupler.*

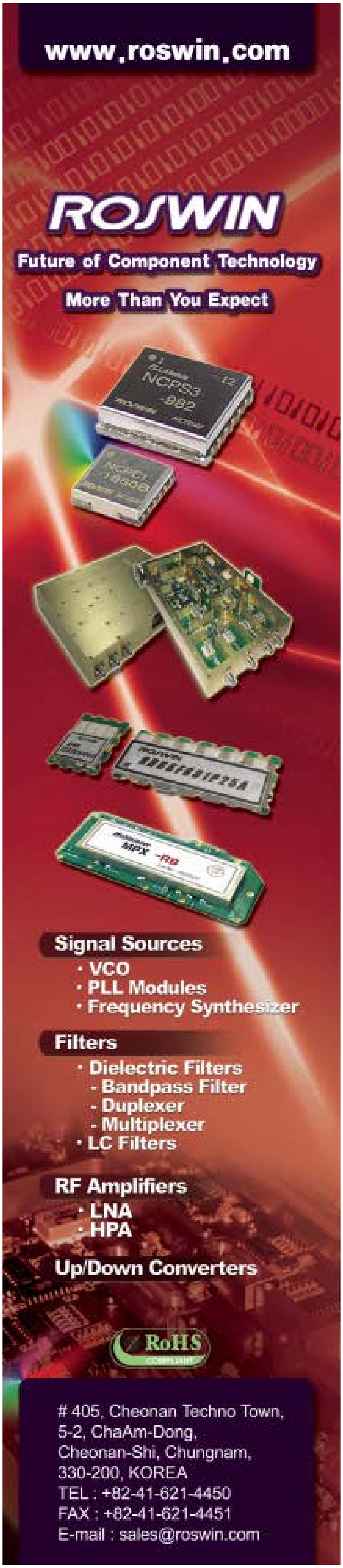
SIMULATION RESULTS

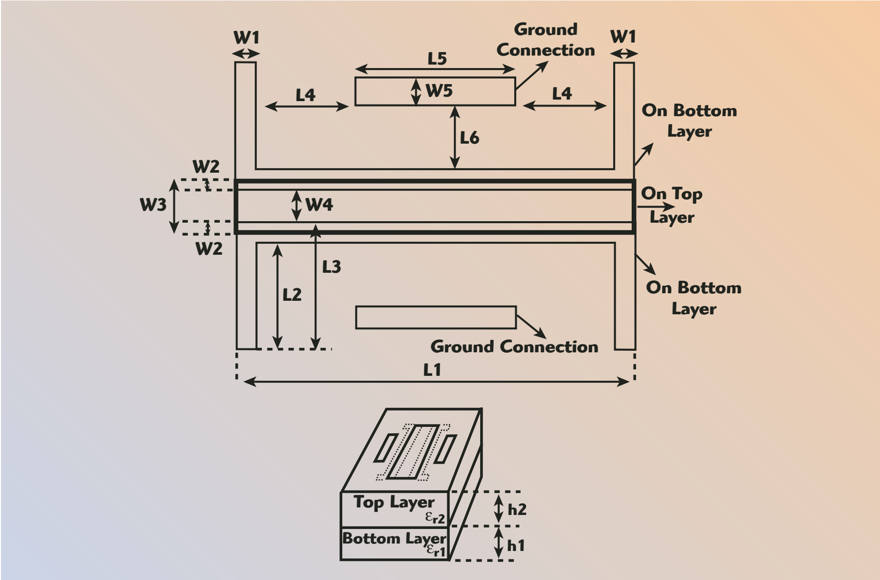
A method of moment-based EM simulation tool was used to simulate the directional coupler. The forward coupling and the directivity levels of the coupler are shown in ***Figure 1***. The simulation results for the forward coupling and the directivity levels at 27.12 MHz are –24.57 and –20.71 dB, respectively. Based on the simulation results, the forward coupling and the directivity levels are found to be –9.51 and –19.76 dB at 300 MHz, respectively.

EXPERIMENTAL RESULTS

The three-line directional coupler was built based on the final parameters obtained by the EM simulator. A photograph of the coupler is shown in ***Figure 2***. The dimensions of the directional coupler are shown in ***Figure 3*** and given in ***Table 1***.

The measured results for the forward coupling and the directivity are shown in ***Figure 4***. The measured results for forward coupling and the directivity levels at 27.12 MHz are –23.03 and –21.69 dB, respectively. The forward coupling and the directivity levels at 300 MHz are found to be –10.05 and –18.21 dB, respectively. There is approximately a four percent error between the measured and the specified forward-coupling levels. The improved directivity response of the coupler seen around the operational frequency is due to the optimization implemented on the structure to get a higher directivity level.



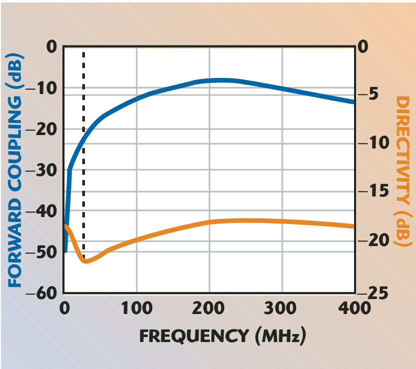


▲ *Fig. 3 Layout of the directional coupler indicating the dimensions.*

TABLE I

DIMENSIONS (IN MILS) OF THE CONSTRUCTED DIRECTIONAL COUPLER

L1	*L2*	*L3*	*L4*	*L5*	*L6*	
7250	1225	1375	2107	2736	646	
W1	*W2*	*W3*	*W4*	*W5*	*h1*	*h2*
150	75	225	75	150	60	60



▲ *Fig. 4 Measured forward coupling and directivity.*

CONCLUSION

A multi-layer three-line directional coupler for high power RF applications in the HF range has been designed, simulated, built and measured. The results show that it is possible to design microstrip directional couplers in the HF range, if the coupler is designed at a higher frequency and its forward-coupling slope characteristic is used to meet the desired coupler specifications. This design technique significantly reduces the physical length of the directional coupler. In addition, it is shown that a multi-layer structure for microstrip directional couplers in the HF range increases their performance and makes them attractive for high power applications, since a multi-layer configuration effectively increases the minimum arcing distance between the main and coupling lines. ■

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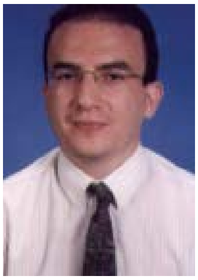

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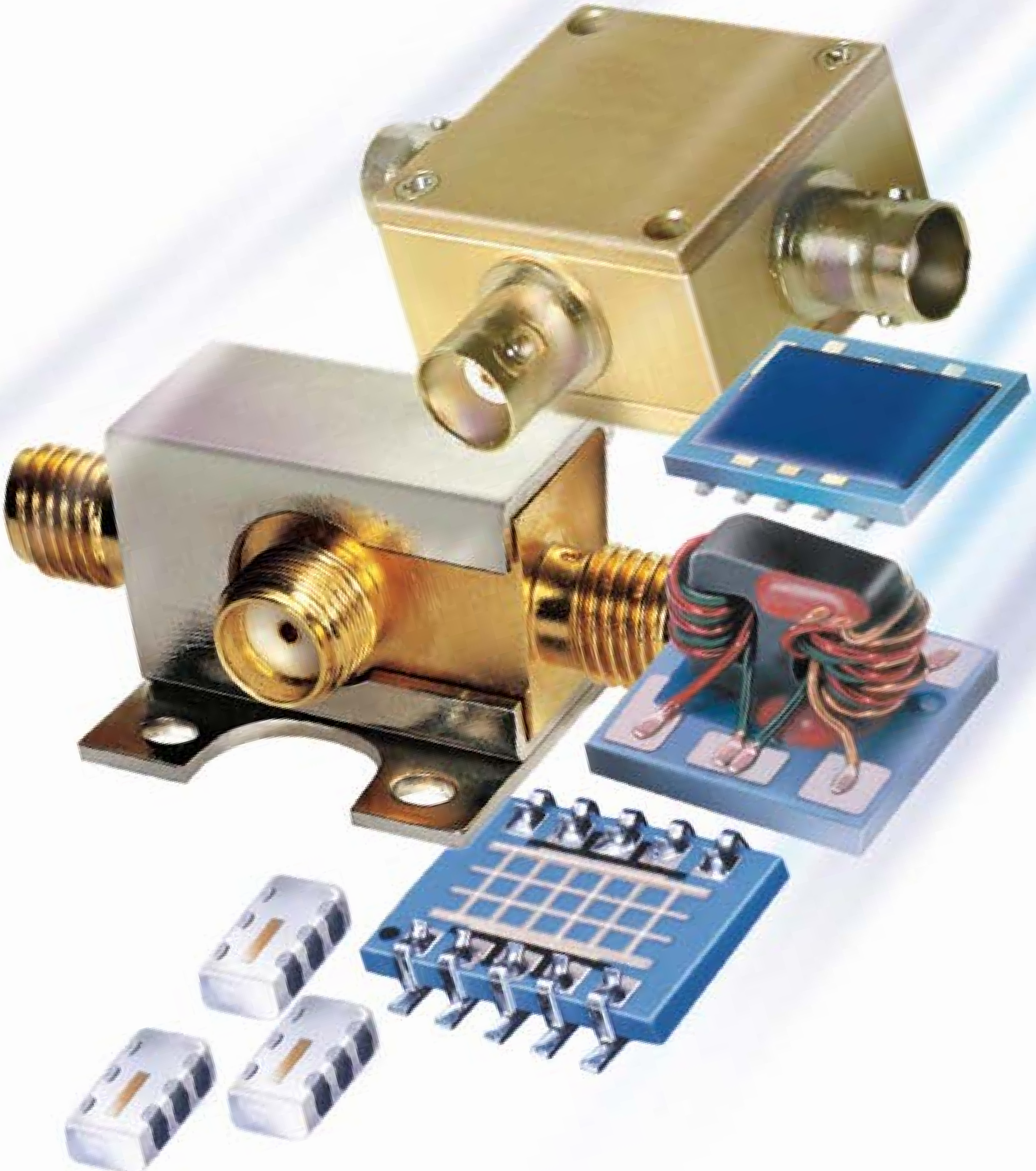
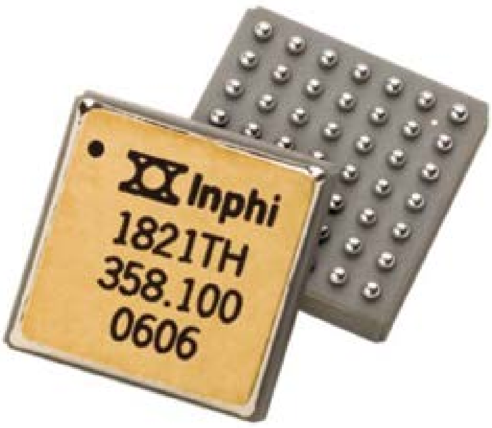


A HIGH SPEED FAMILY OF COMMERCIAL TRACK-AND-HOLD DEVICES FOR ULTRA-WIDEBAND APPLICATIONS



A new class of very high input analog bandwidth and high sampling rate track-and-hold amplifiers (THA) has been developed for test and measurement, automatic test equipment (ATE), digital receivers and radar systems using a commercially available indium phosphide (InP) technology. Inphi® Corp.'s GigaTrack™ family of 2 GS/s track-and-hold amplifiers features an analog input bandwidth of 12 GHz at 1 V_{pp} input and a sampling rate as high as 2 GS/s. The photograph above shows the THA in a ceramic ball-grid-array (BGA) package. These products deliver ultra-wide 18 GHz analog bandwidth. The combined bandwidth, sample rate and linearity of these track-and-holds make direct conversion and software-defined receivers possible, and advance the state-of-the-art in high sample rate test and measurement equipment. The GigaTrack track-and-holds operate from a single –5.2 V power supply and dissipate only 1.3 W. They are available in a 49-pin ceramic ball-grid-array and in 24 pin QFN packages.

InP technology is the fastest semiconductor technology in production today. Because of this inherent advantage, circuits made in InP typically outperform those made in traditional gallium arsenide (GaAs) and silicon germanium (SiGe) for high speed applications. InP technology is also a cost-effective solution for circuits with reasonable complexity up to about 5000 transistors, competing very well with GaAs and SiGe technologies for high speed front-end applications. Inphi Corp., for example, has shipped InP circuits in high volume since 2002, and continues to develop advanced InP products to meet the ever-increasing demands for high performance integrated circuit solutions.

Fast sampling oscilloscopes and direct conversion receivers in radios, radar or electronic warfare systems all demand wider-bandwidth and higher sample rate analog-to-digital con-

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TABLE I

COMPARISON OF GIGAHERTZ-CLASS TRACK-AND-HOLD AMPLIFIERS

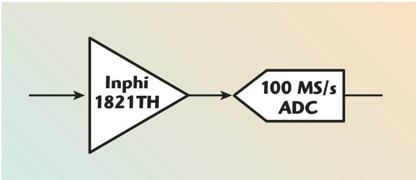
	Inphi InP 1821TH	Competitor GaAs	Competitor SiGe
Input analog bandwidth (small signal) (GHz)	18	9	N/A
Input analog bandwidth (1 V_{pp}) (GHz)	12	6	3.95
Single tone, total harmonic distortion, 1 V_{pp}, 1 GHz (dB)	–60	–59	–54
Single tone, total harmonic distortion, 1 V_{pp}, 5 GHz (dB)	–40	–25	N/A
Maximum sampling clock (GHz)	2	1	3
Power dissipation (W)	1.3	2.4	1.2

version. With the GigaTrack THAs, engineers can, for the first time, replace numerous components in traditional heterodyne receiver architectures with a track-and-hold and a high sample rate analog-to-digital converter (ADC). The resulting receivers are lower power and more compact than traditional heterodyne receivers and provide far more flexibility. Signal processing (that is, down-conversion or channelizing) that was "hard-wired" in heterodyne receivers, can now be performed digitally and can be "software defined." A direct conversion receiver can serve multiple applications with system differentiation occurring in software or firmware.

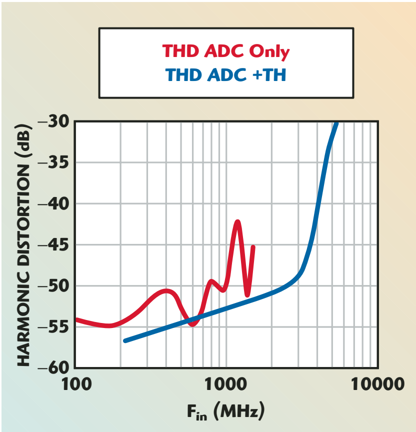
Track-and-hold amplifiers are often used as the high speed front-end of an ADC. The THA's primary function is to track the input signal and hold its voltage constant during the interval required for the ADC to perform the analog-to-digital conversion. By using a high performance THA as the front-end of a low cost commercially available ADC, system designers can extend the input analog bandwidth of the ADC from megahertz to gigahertz frequencies. The resulting circuit offers a significant cost advantage over alternative approaches such as diode bridges and mixers.

High input analog bandwidth, high sampling rate and low harmonic distortion are key parameters for THAs. Existing THAs are made in GaAs and more recently SiGe technology. These devices typically have an input analog bandwidth of 4 to 6 GHz. ***Table 1*** compares the performance of an InP THA (Inphi model 1821TH) against competing products in GaAs and SiGe. The InP THA offers a 12 GHz input analog bandwidth at full swing, 1 V_{pp}, which is an exceptionally high value for any commercial-off-the-shelf THAs today.

Because of the high input analog bandwidth of the InP THA, system designers now can extend the input analog bandwidth of the ADC from around 100 MHz to well over 12 GHz. ***Figure 1*** depicts the block diagram of such a design, in which an InP THA is driving a commercial-off-the-shelf ADC with 100 MHz input analog bandwidth. The resulting circuit offers a significant cost advantage



▲ *Fig. 1 System block diagram of a 12 Gb/s digital sampling scope front-end.*



▲ *Fig. 2 Single-tone total harmonic distortion of the National Semiconductor ADC (model ADC08D1500) with and without the Inphi THA, model 1821TH (external clock F_s=1.5 GHz).*

over alternative approaches and is now in mass production for high speed digital sampling scope and signal analyzer applications.

Another popular application for high input analog bandwidth THAs is for automatic test equipment. At speed testing, it is critical that the high speed signal be captured and digitized in real time. This application requires a very high speed ADC operating at multi-giga samples per second. Such an ADC has recently become available commercially, but its input analog bandwidth is usually not high enough to capture the signal faithfully above 1 or 2 GHz. A high input analog bandwidth THA alleviates this issue, extending the bandwidth of the ADC while improving the overall performance of the system.

As an example, ***Figure 2*** compares the performance of a National Semiconductor high speed ADC (model ADC08D1500) with and without the Inphi THA at a 1.5 GHz sampling clock. Without the Inphi THA, the performance of the ADC, as expected, begins to degrade at input frequencies above 1 GHz, whereas with the Inphi THA, the performance of the combined THA/ADC continues to be excellent up to approximately 3 GHz before experiencing distortion. Five to 10 dB improvements in single-tone total harmonic distortion were obtained with the Inphi THA "front-end" over the entire frequency range from 100 MHz to 3 GHz.

The GigaTrack family consists of four track-and-hold amplifiers with 2 GS/s sample rates. The ball-grid-array versions offer 18 GHz (small signal) and 15 GHz (0.5 V_{pp}) input analog bandwidths with very fast settling times (60 ps) and low power consumption (1.3 W). Plastic QFN versions provide 13 GHz analog bandwidth (100 mV_{pp}).

To deliver a wider hold time window for the downstream ADC, a master/slave (dual) track-and-hold architecture was developed. This provides higher accuracy in the digitization process by increasing the hold time window to almost one full cycle of the THA. For users who want to sub-sample the output of the master track-and-hold with the slave track-and-hold, the 1821TH and lower performance 1321TH devices provide a flexible clock mode select pin which, in one mode, allows the user to provide different clocks to the master and slave track-and-holds.

The GigaTrack family's best-in-class settling time (< 60 ps) maximizes timing margin to improve accuracy and performance, while the best-in-class total harmonic distortion (–70 dB typical at 1 GHz and 500 mV_{pp} input) and aperture jitter (< 50 fs) support improved ADC signal-to-noise-and-distortion ratios leading to more sensitive and accurate acquisition systems. Also, by eliminating the requirement for two separate power supply voltages, these track-and-hold devices simplify board layout, lower system cost and help reduce power consumption by up to 20 percent.

The GigaTrack family supports all popular, broadband analog-to-digital ADC devices including National Semiconductor ADC08100/81500, Atmel AT84AS003/008, ADI 9480, Maxim/Dallas MAX104/108 and others.

In summary, a new class of high input analog bandwidth, high sampling rate GigaTrack THAs is now available for test and measurement, automatic test equipment, digital receivers and radar systems applications. These THAs offer system designers attractive solutions to directly capture and digitize high bandwidth signals at gigahertz frequencies, which result in higher performance, lower cost, smaller size and lower weight systems. Additional information may be obtained from the Inphi GigaTrack web site at www.inphi-corp.com/products/1821th.shtml.

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A 10 TO 20 GHZ SOLID-STATE AMPLIFIER

AR RF/Microwave Instrumentation is introducing a new 5 W solid-state microwave amplifier (SSMA) that operates from AC power. The model 5S10G20 amplifier features high gain, low noise and good linearity making it an excellent replacement for traveling wave tube amplifiers (TWTA). It provides instant power with the press of a button and requires no warm-up time.

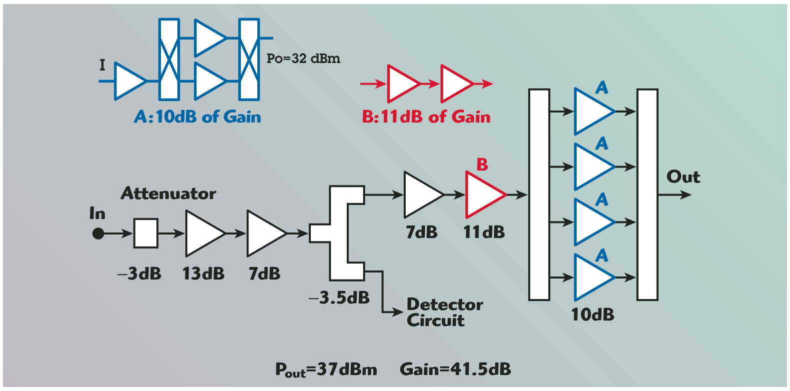
PRODUCT DESCRIPTION

The 5S10G20 solid-state amplifier's block diagram is shown in ***Figure 1***. The design utilizes numerous GaAs FETs and MMICs in a balanced configuration. All devices are biased class A using an active bias circuit. The output stages are combined using AR proprietary technology.

The instrument features a minimum of 5 W output power, 40 dB of gain and a typical noise figure of 6 dB (a significant improvement over a typical TWT amplifier). Gain flatness is within ±1.5 dB across the band, as shown in ***Figure 2***. All second harmonics are better than 20 dBc and the third-order intercept is typically +46 dBm. In addition, the broadband amplifier is protected with an overdrive circuit at the input. ***Figure 3*** shows the amplifier's typical power output characteristics.

The model 5S10G20 amplifier is self-contained, air-cooled and designed for applications where instantaneous bandwidth and high gain are required. Housed in a stylish contemporary cabinet, the unit is designed for benchtop use, but can be removed from the cabinet for equipment rack mounting. When used as a sweep generator, it will provide a minimum of 5 W of RF power. A front panel

Fig. 1 The model 5S10G20 amplifier's block diagram.



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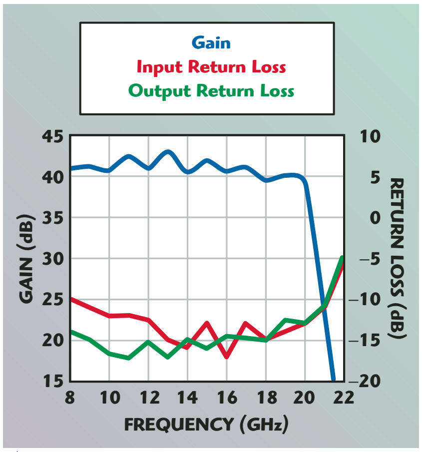
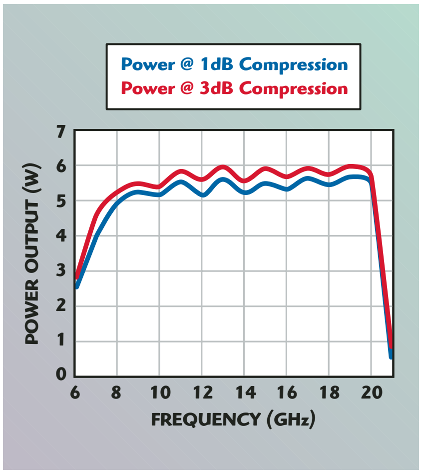


▲ *Fig. 2 Gain and return loss characteristics.*



▲ *Fig. 3 Typical power output.*

gain control is included that permits the operator to conveniently set the desired output level.

The new amplifier is protected from RF overdrive by an RF input leveling circuit that controls the input level applied to the first stage of amplification when the RF input is increased above 0 dBm. In addition, the individual RF amplifier stages are protected from over temperature by removing the DC voltage applied to them if an over temperature condition occurs due to a cooling blockage or fan failure. There is a digital display on the front panel to indicate the operational status and fault conditions when an over-temperature or power supply fault has occurred. The unit can subsequently be returned to normal operation when the condition has been cleared.

The 5S10G20 amplifier includes a digital control for both local and remote control of the amplifier. This eight-bit RISC microprocessor-controlled board provides both IEEE-488 (GPIB) and asynchronous, full duplex RS-232 control of all amplifier functions. ***Table 1*** lists the model 5S10G20 amplifier's electrical specifications.

TABLE I

MODEL 5S10G20 SPECIFICATIONS

Rated power output (W)	5 minimum
Power output @3 dB compression (W) nominal minimum	 7 5
Power output @1 dB compression (W) nominal minimum	 6 5
Gain flatness (dB)	±2.0 typical; ±3.0 maximum
Frequency response (GHz)	10–20 instantaneously
Input for rated output (dBm)	0 max
Gain (at maximum setting) (dB)	40 minimum
Gain adjustment (continuous range) (dB)	10 minimum
Input impedance (Ω)	50, VSWR 2.5:1 maximum
Output impedance (Ω)	50, nominal
Mismatch tolerance	100% of rated power without foldback. Will operate without damage or oscillation with any magnitude and phase of source and load impedance.
Modulation capability	will faithfully reproduce AM, FM or pulse modulation appearing on the input signal
Harmonic distortion (dBc)	–20 maximum at 5 W
Third-order intercept point (dBm)	43 typical
Primary power (selected automatically)	90–132, 180–264 VAC 50/60 Hz, single phase < 550 W maximum

ADVANTAGES OVER TWTAS

AR RF/Microwave Instrumentation manufactures high grade microwave and millimeter-wave amplifiers based on a hybrid thin film and GaAs chip technology. Compared to TWT amplifiers, solid-state amplifiers offer significant advantages over TWTAs in similar applications. As the tube in a typical TWTA ages, the output power continually decreases and readjustment is required. Eventually the tube will need to be replaced. On the contrary, solid-state microwave amplifiers do not require readjustment. The SSMA will outlast the TWTA. The average mean time between failure (MTBF) for a SSMA is greater than 20 years, while the MTBF for a TWT has an average of eight years.

The SSMA is more cost effective than a TWTA. The amplifier provides good linearity for low power levels up to P1dB. Meanwhile, the dynamic range of a TWT amplifier is less than the SSMA because of its noise floor at low power levels, and its harmonics and spurious outputs at high power levels. In conclusion, the SSMA provides a much cleaner, more stable output and better intermodulation performance.

AR RF/Microwave Instrumentation, Souderton, PA (215) 723-8181, www.ar-worldwide.com.

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Model	Freq. (MHz) f_L - f_U	Gain (dB) Typ.	Max. P_{OUT} (dBm) @ Compression 1 dB	3 dB	Dynamic Range NF (dB) Typ.	IP3 (dBm) Typ.	DC Pwr. Volt (V) Nom.	Current (A) Max.	Price $ea. Qty. 1-9
With Heat Sink/Fan									
ZHL-5W-2G	800-2000	49	+37	+38	8.0	+44	24	2.0	995.00
ZHL-10W-2G	800-2000	43	+40	+41	7.0	+50	24	5.0	1295.00
• ZHL-20W-13	20-1000	50	+41	+43	3.5	+50	24	2.8	1395.00
• ZHL-50W-52	50-500	50	+46	+48	4.0	+55	24	9.3	1395.00
• ZHL-100W-52	50-500	50	+47	+48.5	6.5	+57	24	9.3	1995.00
▲ ***Without Heat Sink/Fan***									
ZHL-5W-2GX	800-2000	49	+37	+38	8.0	+44	24	2.0	945.00
• ZHL-10W-2GX	800-2000	43	+40	+41	7.0	+50	24	5.0	1220.00
• ZHL-20W-13X	20-1000	50	+41	+43	3.5	+50	24	2.8	1320.00
• ZHL-50W-52X	50-500	50	+46	+48	4.0	+55	24	9.0	1320.00
• ZHL-100W-52X	50-500	50	+47	+48.5	6.5	+57	24	9.0	1920.00

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▲ *With heat sink/fan removed, customer must provide adequate cooling to ensure that the base plate temperature does not exceed 85°C.*
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416 Rev D

AN ULTRA-LOW NOISE VHF OCXO

Over the past 50 years crystal oscillators have become ubiquitous wherever a stable reference is needed in RF systems. The new Pascall OCXO has been developed to address the most critical applications where ultra-low noise is required; for example, as a reference for phase noise measurement, or as the master oscillator in radar systems or low noise frequency multipliers/synthesizers.

PHASE NOISE

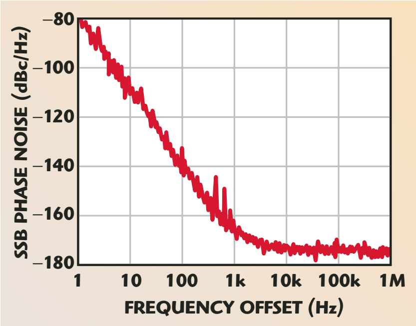
In order to better understand the OCXO's development, consider the factors affecting phase noise, starting with the fact that if an oscillator is considered as a feedback amplifier combined with a resonator, Leeson's model predicts that the close-to-carrier noise is determined by the signal level, the amplifier's noise figure and the Q of the resonator. Assuming the signal is taken from the amplifier output, the single-sideband (SSB) noise density at a given offset is the amplifier's noise floor plus the noise floor multiplied by a –20 dB/decade slope, with the two curves intersecting at the resonator's half bandwidth. (At offsets lower than the amplifier's flicker corner frequency, the slope is –30 dB/decade.)

In real oscillators, the steady-state loop gain is maintained at unity by either limiting or automatic gain control (AGC) action. This has the effect of suppressing AM noise, which typically shows a –10 dB/decade slope below the amplifier's flicker corner frequency.

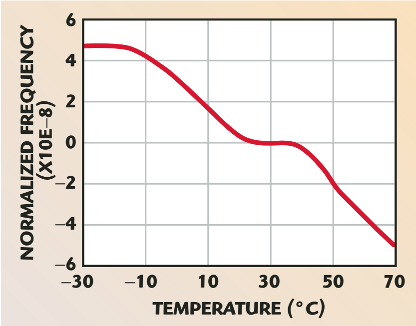
Crystal oscillators generally have much worse phase noise than the Leeson model predicts. This is because the resonators themselves exhibit 1/f FM noise, which translates to $1/f^3$ phase noise. In low noise oscillator designs, the close-to-carrier noise is generally dominated by the crystal's noise rather than its loaded Q or the circuit noise. Crystal selection is essential if low phase noise is important, as there can be more than 20 dB variation even within a single batch of crystals.

High Q is still important, as it reduces the oscillator circuit's contribution to close-in noise, and minimizes supply pushing and load pulling. At frequencies around 100 MHz, fifth overtone SC-cut crystals offer the best combination of low noise and high Q, together with a flat frequency/temperature characteristic at their turnover point, typically about 80°C.

PASCALL ELECTRONICS LTD.
Ryde, Isle of Wight, UK



▲ *Fig. 1 Uncorrected phase noise of a pair of OXCOs at 100 MHz.*



▲ *Fig. 2 Frequency drift from -30° to +70°C.*

At higher offsets, the noise is determined by the drive level and the circuit's noise floor. SC-cut crystals generally allow higher drive levels to be used than AT-cut. Taking the oscillator output via the resonator utilizes the filtering action of the crystal, so that only the output buffer contributes to the noise floor.

It is important to operate the active devices linearly if the full potential of the lowest noise crystals is to be realized. Nonlinear operation generally increases the transistors' flicker noise and also causes modulation of the signal by power supply noise and ripple. The degree of degradation tends to vary with factors such as crystal motional resistance and temperature.

Linear operation also helps when tuning the oscillator, as SC-cut crystals in particular need large series reactance to tune them away from series resonance. If the RF operating conditions are not well defined, the tuning range may be limited by wide variation in output power and/or unwanted oscillation modes, particularly with the drive levels needed for low noise floor.

DESIGN CONSIDERATIONS

Practical oscillator design almost always involves compromises and tradeoffs. The Pascall OCXO aims to provide the lowest possible phase noise within a relatively compact 2" × 2" × 0.75" package.

A low noise regulator is followed by further filtering and careful attention is paid to ground paths, in order to minimize the effect of supply noise and prevent oven current noise affecting the oscillator's performance. Fairly high signal levels must be used in order to achieve a very low noise floor. In combination with the linear operation required for lowest possible close-in noise, this inevitably results in higher dissipation than in oscillators with lower performance.

To ensure good temperature control up to 70°C, the oven needs to be maintained at ~80°C. In the great majority of applications, the oscillator will not need to be operated continuously at its maximum temperature. In order to maximize reliability and reduce oven power requirements, only the crystal and certain critical components are held at 80°C. A temperature compensation circuit minimizes drift due to the oscillator circuit.

The Pascall standard part is designed to operate with base plate temperatures of –30° to +70°C. Alternative temperature ranges are available, down to –40°C and up to 85°C. The supply voltage is +12 V, while +15 V is available as an option.

The new OCXO has a relatively wide tuning range, to give ample allowance for aging or locking to external references. At 100 MHz the range is typically ±10 ppm for 0 to 10 V input, with virtually no change in phase noise across the range. The standard oscillator has electrical tuning. It is also available with internal mechanical tuning, or a reference voltage output can be provided to enable the oscillator to be tuned by an external potentiometer.

TYPICAL PERFORMANCE

Figure 1 shows a phase noise plot of a pair of OCXOs at 100 MHz. This is an uncorrected plot, and therefore shows the combined noise of two oscillators. The noise floor measurement is limited by the test system noise, which is actually higher than the oscillator's noise floor. (Accurate measurement of very low noise is always a difficult exercise.) Allowing for the test system noise and subtracting 3 dB for the two-oscillator measurement shows the OCXO's phase noise floor to be ~–180 dBc/Hz per oscillator.

The best-selected crystals have been found to yield well under –140 dBc/Hz at 100 Hz offset from 100 MHz. However, it is important not to over specify when designing an OCXO into a system, as this will have a major impact on cost. As previously stated, a crystals' phase noise varies widely even within a single batch, so careful screening is necessary to meet the most stringent specifications. Also, reliable measurement of low phase noise is very time consuming. The new unit's output power is 13 dBm ±2 dB into 50 Ω and harmonics are ≤–20 dBc.

The total frequency drift from –30° to +70°C is typically ~1 × 10^{-7} (see ***Figure 2***). Warm-up power is typically 5 W and the steady-state power at 25°C is ~2.5 W. There is always a tradeoff between operating temperature range and power consumption. Specifying a higher maximum temperature will increase the consumption at all temperatures, as the oven must be held a few degrees above the highest working ambient temperature. Reducing the minimum operating temperature will increase the warm-up current, as the heater must be able to maintain a larger differential between oven and ambient temperature.

CONCLUSION

The new OCXO addresses the most critical applications where ultra-low noise is required and aims to provide the lowest possible phase noise within a compact package. It features a relatively wide tuning range and a temperature compensation circuit.

As for the future, Pascall is now well into development of a vibration-isolated variant. This unit utilizes low-g-sensitivity crystals and elastomer AV mounts to reduce the influence of shock and vibration on phase noise. This new unit will be suited to fast jet and helicopter vibration and environmental requirements.

**Pascall Electronics Ltd.,
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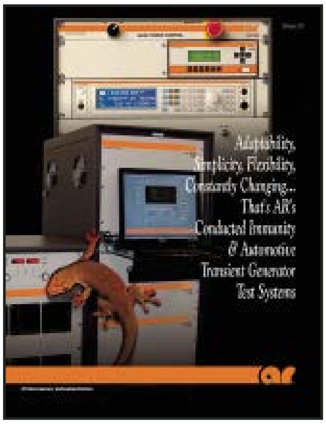

Systems Brochure

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Product Catalog

The "What's New at AVX" catalog highlights more than 18,000 new parts and 60 new product families introduced in 2006. The catalog includes new capacitors, circuit protection, filters, RF/microwave, integrated passives, resistive devices, timing devices, module devices and connectors that provide design solutions for a wide variety of applications. The catalog contains 62 product families as well as details on new software and literature.

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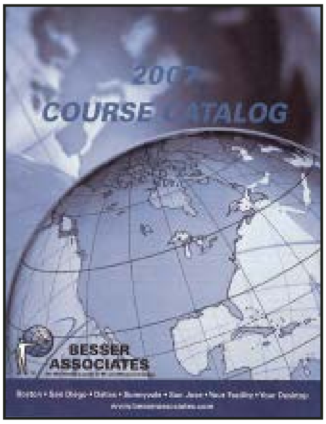

Course Catalog

The 2007 General Course catalog includes detailed outlines of over 100 specialized training courses available to professionals in the RF and wireless industry. Instructor biographies are included as well as a listing of courses grouped by subject area. All courses can be ordered for presentation at individual company facilities.

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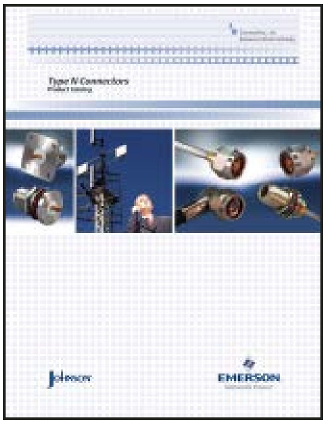

Product Catalog

This catalog features the company's Johnson® Type N connectors that meet or exceed the performance requirements of MIL-PRF-39012. All designs are based on a 50 Ω system impedance per MIL-STD-348 and operate at frequencies up to 11 GHz minimum. All contacts are plated with 50 micro-inches of gold for good durability and high frequency performance. Applications include: antennas, base stations, cable assemblies, microwave radio, RF and microwave components.

Emerson Network Power Connectivity Solutions, Johnson Division,
Waseca, MN (800) 247-8256,
www.emersonnetworkpower.com/connectivity.

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Product Brochure

This product catalog details the company's design and production of a complete line of voltage-controlled oscillators in a variety of packages that cover the frequency range of 5 MHz to 12 GHz. The intra-company design standards set for the military grade product line carry over to the commercial product line providing a rugged unit capable of withstanding vibration, shock, temperature and other environmental extremes.

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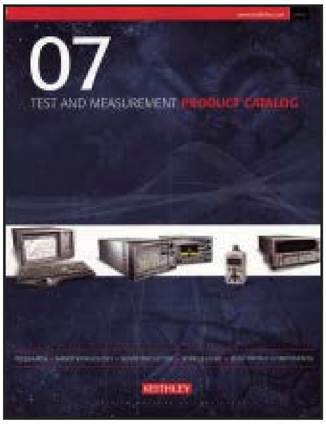

Product Catalog

The 2007 test and measurement product catalog serves as a desktop reference guide that offers details and specifications on the company's general-purpose and sensitive sourcing and measurement products, DC switching, RF switching and measurement, data acquisition solutions, semiconductor test systems and optoelectronics test hardware. Tutorials simplify choosing solutions for specific applications. To request a free copy of the 2007 catalog, visit www.keithley.com/pr/065.

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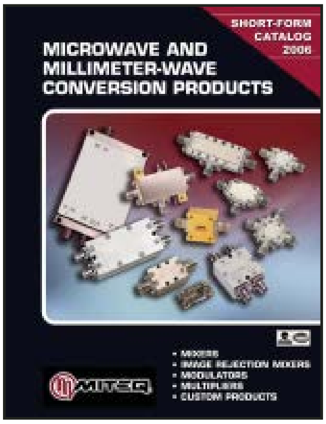

Short Form Catalog

The microwave and millimeter-wave conversion products short-form catalog features a sampling of the company's latest state-of-the-art mixers, image rejection mixers, modulators, multipliers and custom products. There are also sections discussing quality assurance, manufacturing flow diagrams, MITEQ's Space Heritage and options available to the customer.

MITEQ,
Hauppauge, NY (631) 436-7400, www.miteq.com.

RS No. 318

Product Selection Guide

This product selection guide features the company's precision, high frequency connectors and adaptors that operate in a frequency range from DC to 50 GHz. The brochure provides selection tables that include electrical and mechanical specifications for the new 2.4 mm, 2.92 mm and 3.5 mm, precision SMA and SSMA families. Connectors are available in flanges or thread-in configurations. A family of push-on adaptors in N, SMA, 2.4, 2.92 and 3.5 is offered to facilitate testing in lab environments.

Response Microwave Inc.,
Framingham, MA (978) 456-9184,
www.responsemicrowave.com.

RS No. 319

Solutions Guide

The RF cable assembly solutions guide features three easy steps to building cables. WiFi connectors are indicated. RF Cable Assemblies division of RF Industries (RFI) offers custom coaxial cable assemblies. It also fabricates a full line of standard cable assemblies, shown in the RF Connectors Catalog. A connector ID chart is also included in the solutions guide. The guide is also available on a CD-ROM.

RF Industries,
San Diego, CA (858) 549-6340, www.rfindustries.com.

RS No. 320

Selection Guide

This 36-page product selection guide features new RF products for existing and emerging RF markets, and catalog parts ranging from signal source and signal processing components, and the company's amplifiers—which include patented active-bias gain blocks, LNAs, award-winning WiMAX amplifiers, LDMOS and others. Also look for new passive devices from Premier Devices and new ISM transceiver and networking solutions from Micro Linear.

Sirenza Microdevices,
Broomfield, CO (303) 327-3030, www.sirenza.com.

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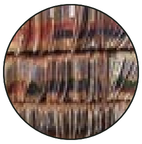

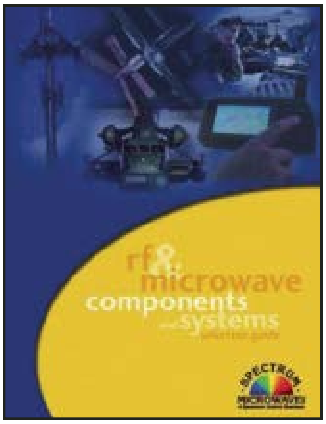

Product Selection Guide

This selection guide highlights the various products from recent acquisitions of Amplifonix, FSY Microwave, Magnum Microwave, Q-bit, Salisbury Engineering and Radian Technologies. Products covered include RF amplifiers, power amplifiers, mixers, VCOs/DROs and attenuators. Featured microwave filters include lumped element, waveguide, tubular and cavity filters, and suspended substrates. Microwave systems include integrated assemblies, switched filter banks, frequency multipliers and synthesizers.

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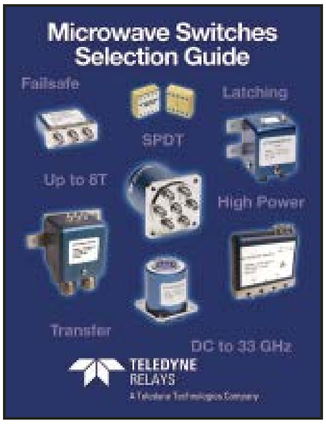
RS No. 327

Product Brochure

This brochure has been updated to reflect the expansion of the extra-durable Storm Flex™ miniature cable line to include a larger, 0.160" diameter cable that is a high strength flexible replacement for RG-402 semi-rigid cable. Mechanical, electrical product specifications; competitive analysis graphs for VSWR, phase, insertion loss vs. flexure; applications; and complete ordering information are also included.

Storm Products–Microwave,
Woodridge, IL (630) 754-3300,
www.stormproducts.com/microwave.

RS No. 322



Selection Guide

The microwave switches selection guide features 20 families of coaxial switches and relays in a tabular format. The guide, designed to help engineers quickly choose a product, now features schematic drawings for all switches and relays. The 24-page digest provides detailed information about the switches and relays, which span the range from DC to 26.5 GHz and cover SPDT up to SP8T and transfer switches.

Teledyne Relays,
Hawthorne, CA (800) 284-7007, www.teledynerelays.com.

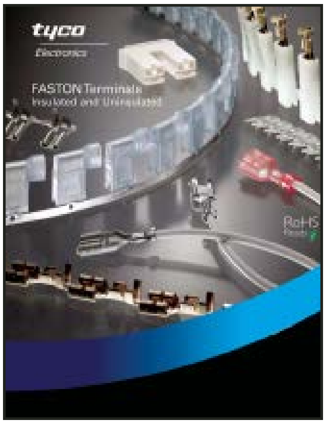
RS No. 323

Capabilities Brochure

This brochure details how Terabeam/HXI and BTP Systems have joined forces to provide customers the best choice for repair and refurbishment of complete radar, RF communications and SATCOM systems. Collectively, its employees have served this industry successfully for over 30 years. This repair and refurbishment vendor possesses a high level of skills in electromechanical, RF, microwave and millimeter-wave systems.

Terabeam/HXI,
Haverhill, MA (978) 521-7300, www.terabeam-hxi.com.

RS No. 324

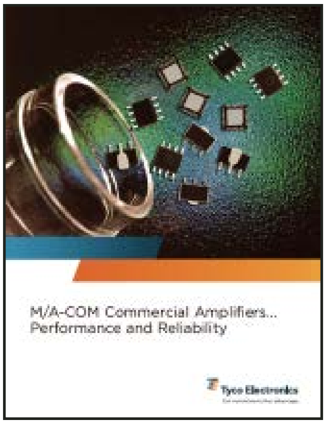


Product Catalog

This catalog provides the latest technical information and a comprehensive listing of the company's robust line of quick connect electrical terminals. FASTON quick connect electrical terminals are a popular connection method for a number of OEM electronics applications in a wide range of industries. FASTON quick connect electrical terminals are used extensively in industrial and commercial electronics for power connections in wire harnesses and printed circuit boards.

Tyco Electronics Corp.,
Harrisburg, PA (800) 522-6752, www.tycoelectronics.com.

RS No. 325



Commercial Amplifiers Brochure

The Tyco Electronics M/A-COM commercial amplifier brochure covers the most widely used plastic packaged solutions for wireless applications such as WiMAX, WLAN, cellular infrastructure, RFID, cordless and mobile. It contains an easy to use selection guide sorted by frequency with full parametric data.

Tyco Electronics M/A-COM,
Lowell, MA (800) 366-2266, www.macom.com.

RS No. 326

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New listings offering hundreds of new models.

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Ultra Broadband

Freq. Range (GHz)	Gain (dB)	Gain Flatness (+/- dB)	NF (dB)	OP1dB (dBm)	OIP3 (dBm)	VSWR In/Out	Max. CW RF Input (dBm)	DC Current @ +12VDC (mA)	Model Number	Cost ($ USD) 1-10	11-20	20+
0.03-20	14	2.5	3.0	14	26	2.0:1	23	75	PUB-14-30M20G-14-LCA	850	750	650
0.03-20	15	2.5	3.0	20	30	2.0:1	23	180	PUB-15-30M20G-20-LCA	950	850	750
0.50-20	14	1.75	3.0	14	26	2.0:1	23	75	PUB-14-500M20G-14-LCA	750	650	550
0.50-20	15	1.75	3.0	20	30	2.0:1	23	180	PUB-15-500M20G-20-LCA	850	750	650

Broadband

Freq. Range (GHz)	Gain (dB)	Gain Flatness (+/- dB)	NF (dB)	OP1dB (dBm)	OIP3 (dBm)	VSWR In/Out	Max. CW RF Input (dBm)	DC Current @ +12VDC (mA)	Model Number	Cost ($ USD) 1-10	11-20	20+
2-20	15	1.75	3.0	12	24	2.0:1	23	75	PBB-15-220-12-LCA	750	650	550
2-20	28	2.25	3.0	12	24	2.0:1	23	150	PBB-28-220-12-LCA	850	750	650
2-18	10	1.75	4.0	16	28	2.0:1	23	75	PBB-10-218-16-LCA	650	550	450
2-18	15	2.0	3.0	20	30	2.0:1	23	180	PBB-15-218-20-LCA	800	700	600
2-18	20	2.0	4.0	16	28	2.0:1	23	150	PBB-20-218-16-LCA	800	700	600
2-18	28	2.5	3.0	20	29	2.0:1	23	250	PBB-28-218-20-LCA	850	750	650

Octave Band

Freq. Range (GHz)	Gain (dB)	Gain Flatness (+/- dB)	NF (dB)	OP1dB (dBm)	OIP3 (dBm)	VSWR In/Out	Max. CW RF Input (dBm)	DC Current @ +12VDC (mA)	Model Number	Cost ($ USD) 1-10	11-20	20+
2-4	10	1.0	4.0	10	18	2.0:1	10	75	POB-10-24-10-LCA	450	350	300
2-4	15	1.0	3.5	15	26	2.0:1	23	75	POB-15-24-15-LCA	500	450	350
2-4	17	1.0	3.5	22	34	2.0:1	23	180	POB-17-24-22-LCA	550	450	400
2-4	28	1.25	3.5	15	26	2.0:1	23	150	POB-28-24-15-LCA	550	450	400
4-8	10	1.0	3.0	10	18	2.0:1	10	75	POB-10-48-10-LCA	450	350	300
4-8	15	1.0	3.0	15	26	2.0:1	23	75	POB-15-48-15-LCA	500	450	350
4-8	16	1.0	3.0	22	32	2.0:1	23	180	POB-16-48-22-LCA	550	450	400
4-8	28	1.25	3.0	15	26	2.0:1	23	150	POB-28-48-15-LCA	550	450	400
8-18	10	1.5	3.0	8	16	2.0:1	10	75	POB-10-818-8-LCA	600	500	400
8-18	15	1.5	3.0	13	25	2.0:1	23	75	POB-15-818-13-LCA	650	550	450
8-18	15	1.75	3.0	20	26	2.0:1	23	180	POB-15-818-20-LCA	700	600	500
8-18	28	1.75	3.0	13	24	2.0:1	23	150	POB-28-818-13-LCA	750	650	550

Low Noise

Freq. Range (GHz)	Gain (dB)	Gain Flatness (+/- dB)	NF (dB)	OP1dB (dBm)	OIP3 (dBm)	VSWR In/Out	Max. CW RF Input (dBm)	DC Current @ +12VDC (mA)	Model Number	Cost ($ USD) 1-10	11-20	20+
1-2	18	1.0	1.5	15	28	2.0:1	0	65	PLN-18-12-15-LCA	500	400	300
2-4	18	1.0	1.5	15	28	2.0:1	0	65	PLN-18-24-15-LCA	550	450	350
4-8	17	1.25	1.75	15	28	2.0:1	0	65	PLN-17-48-15-LCA	600	500	450
6-8	32	1.25	1.0	2	10	2.0:1	10	40	PLN-32-68-2-LCA	650	550	450
8-10	32	1.25	0.8	2	10	2.0:1	10	40	PLN-32-810-2-LCA	650	550	450
8-12	25	1.0	1.8	10	18	2.0:1	20	75	PLN-25-812-10-LCA	700	600	500
10-12	30	1.5	0.8	2	10	2.0:1	10	40	PLN-30-1012-2-LCA	650	550	450
1-10	17	1.5	2.0	15	28	2.0:1	0	65	PLN-17-110-15-LCA	750	700	650

Planar Electronics Technology & Planar Filter Company - (A division of Planar Electronics Technology, Inc.)
Phone: 1.877.PLANAR1 • 301.662.5019 • FAX: 301.662.1731 • 5715 Industry Lane, Unit 11, Frederick, MD 21704
Email: PET-SALES@planarelec.com • Web: www.planarelec.com/04 * Check out web for Terms and Conditions of Sale.

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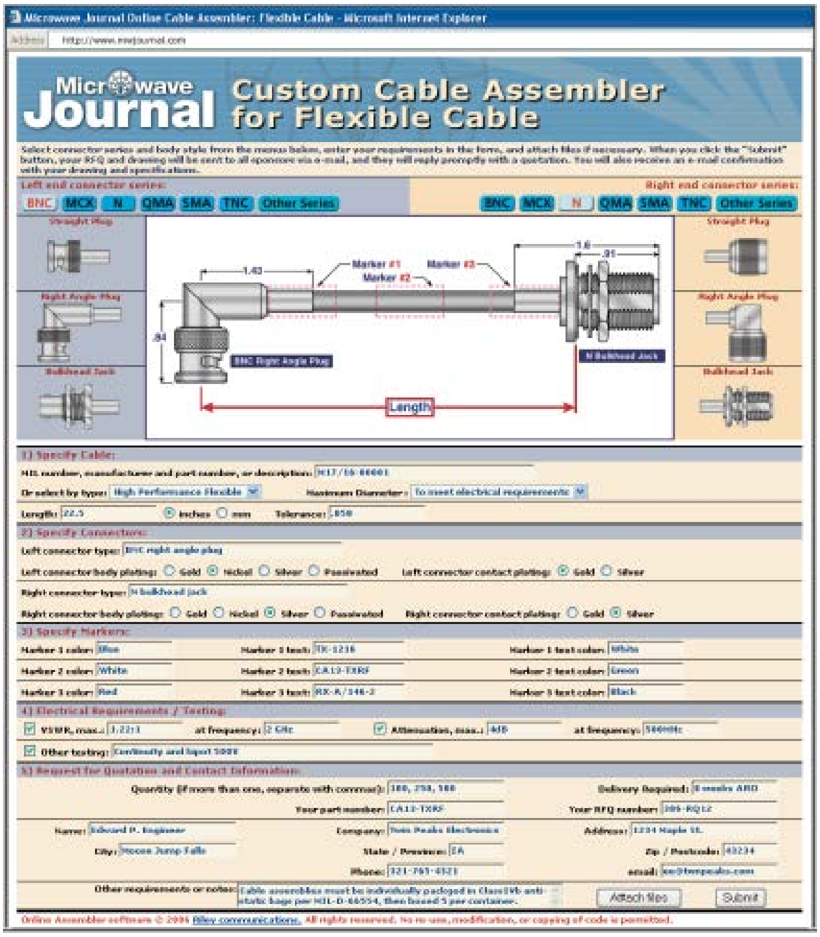

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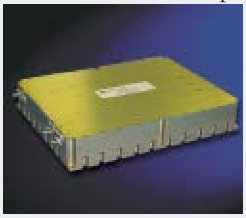
GaN Broadband Power Amplifier

The model SSPA 0.5-3.0-50 is a high power, broadband, GaN RF amplifier that operates in a frequency range from 0.5 to 3 GHz. This PA is ideal for broadband military platforms as well as commercial applications because it is robust and offers high power over a multi-octave bandwidth. This amplifier was designed for broadband jamming and communication systems platforms. This amplifier operates with a base plate temperature of 85°C with no degradation in the MTBF for the GaN devices inside. The RF line up is comprised of all GaN devices. This amplifier has a minimum P3dB of 50 W at room temperature. Size: 7" × 9" × 1.5".



Aethercomm Inc.,
San Marcos, CA (760) 598-4340,
www.aethercomm.com.

RS No. 216

Successive Detection Log Video Amplifier

The model SDLVA-61F-80-582987-004 option TBRK, MS is a matched set of successive detection log video amplifiers in a compact stacked configuration. This unit operates over 61.25 MHz ±250 kHz with a transfer function of E – 22.5 P_{IN}+ 200, where P_{IN} is the input power in dB above –80 dBm and E = output voltage in millivolts. The unit has been designed so that both modules share a common power terminal.

Planar Monolithics Industries Inc.,
Frederick, MD (301) 631-1579,
www.planarmonolithics.com.

RS No. 221

Broadband Power Amplifier

The model QPJ-02064230-A0 is a 2 to 6 GHz, 15 W broadband power amplifier that utilizes unique power combining techniques to deliver 15 W (+42 dBm) output power with flatness of ±0.50 over the 2 to 6 GHz frequency range. The measured gain of this amplifier is 33 dB minimum with gain flatness of ±1.50 dB over 2 to 6 GHz. The amplifier resides in a housing of 2.50" × 1.75" × 0.50" and the RF connectors are removable SMA(F).

QuinStar Technology Inc.,
Torrance, CA (310) 320-1111,
www.quinstar.com.

RS No. 222

Upgrade Existing Amplifiers

This new concept called "Subampabilty" enables labs to upgrade their existing "S" series (1 to 800 W, 0.8 to 20 GHz) amplifiers to higher power without purchasing new amplifiers. Once an initial upgrade is performed, the sky's the limit. Models 20S4G11A (20 W, 4 to 10.6 GHz) and 35S4G8 (35 W, 4 to 8 GHz) are building blocks that can easily be expanded by adding sub amps and controller/combiner units. The 20S4G11A can expand to 40, 60 or 80 W, while the 35S4G8 can grow to 60, 90 or 120 W.

AR RF/Microwave Instrumentation,
Souderton, PA (215) 723-8181,
www.ar-worldwide.com.

RS No. 217

Solid-state Power Amplifier

The model BM2719-80 is a class AB linear amplifier that operates over the full 20 to 1000 MHz frequency range with output power of 80 W. The amplifier is compact (6.4" × 3.4" × 1.06") and weighs only 1 pound.

Comtech PST,
Melville, NY (631) 777-8900,
www.comtechpst.com.

RS No. 218

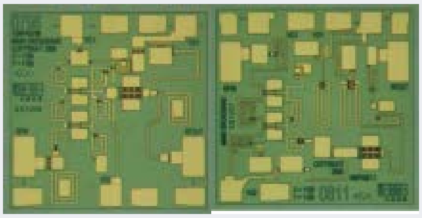
RF Amplifiers

The JCA line of RF amplifiers includes over a dozen models with an average gain tracking of ±0.75 dB and ±1.5 dB gain matching across a 2 to 18 GHz bandwidth. The high performance and reliability of these amplifiers is primarily achieved as a result of an automated assembly process using precise pick-and-place machinery and automatic wire-bonding. Minimizing gaps between components and maintaining efficient, consistent wirebond lengths in the assembly process yields significantly improved gain and phase tracking performance unit-to-unit, and often reduces RF tuning times by 30 percent.

Endwave Defense Systems,
Sunnyvale, CA (408) 522-3180,
www.endwave.com.

RS No. 219

GaAs MMIC Buffer Amplifiers



Models XB1007-BD and XB1008-BD are GaAs MMIC two-stage buffer amplifiers. Using 0.15 micron gate length GaAs PHEMT device model technology, these buffer amplifiers cover 4 to 11 GHz and 10 to 21 GHz, respectively. Both devices deliver +20 dBm P1dB compression point and +30 dBm OIP3. The XB1007-BD has a noise figure of 4.5 dB and 23 dB small-signal gain; the XB1008-BD has a noise figure of 5.5 dB and 18 dB small-signal gain. These buffer amplifiers are ideal for wireless communications applications such as millimeter-wave point-to-point radio, local multipoint distribution services (LMDS), SATCOM and VSAT applications.

Mimix Broadband Inc.,
Houston, TX (281) 988-4600,
www.mimixbroadband.com.

RS No. 220

High Stability OCXOs

These rad-hardened oven-controlled crystal oscillators (OCXO), with a radiation tolerance of up to 1 G, are designed for use in a variety of industrial and military applications. Using proprietary compensation and stabilization methods, the OCXOs can maintain a frequency stability of 1 ppb over a wide operating temperature range of –55° to +85°C. Customers can specify sine wave, HCMOS, TTL or PECL output; a frequency range of 1 MHz to 120 MHz; and an input of 3.3, 5, 12 and 15 V. Custom frequencies and input voltages are also available.

MMD Components,
Rancho Santa Margarita, CA
(949) 753-5888, www.mmdcomp.com.

RS No. 247

Ultra-low Noise Oscillator

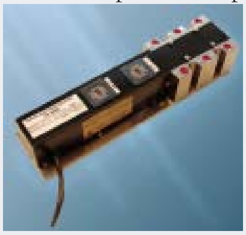
The SR W150 ultra-low phase noise RF oscillator comes in a 51.5 by 51.5 by 20.5 mm package and is designed for the instrumentation and radar markets. It exhibits many technical state-of-the-art characteristics including a frequency of 500 MHz, with frequencies possible from 300 to 600 MHz. The frequency is stabilized by temperature control and an external control voltage. Other characteristics include a low phase noise of –165 dBc/Hz at 10 kHz from the carrier and a phase noise floor of –175 dBc/Hz. Stability is 1 ppm in the 0° to 50°C temperature range with a target of –30°C to +70°C. Once adjusted in the factory, the oscillator never requires any additional calibration.

Temex,
Sophia-Antipolis, France
+33 (0) 4 97 23 30 00, www.temex.com.

RS No. 223

Mini TWT for SATCOMs

The TH 4080 mini traveling wave tube has been developed to incorporate a transmitter amplifier for Very Small Aperture Terminal (VSAT) light SATCOM mobile systems. It is designed for both commercial and military applications that require up to 150 W peak power. It operates in the Ka-band at 27.5 to 31 GHz and its lightweight, compact design and wide bandwidth make it an ideal solution for portable mobile systems. The device applies the proven technology of the company's TH 4062, TH 4072 and TH 4082 families of high power TWTs for satellite uplinks and meets military standards for vibration, shock and temperature.

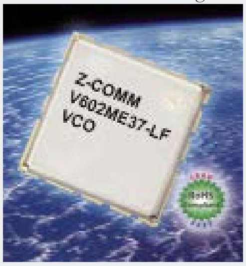


Thales Electron Devices,
Velizy, France +33 (0) 1 3070 3500,
www.thalesgroup.com/electrondevices.

RS No. 224

L-band Voltage-controlled Oscillator

The model V602ME37-LF is an L-band (1300 to 1600 MHz) voltage-controlled oscillator (VCO) that offers a low phase noise performance of –100 dBc/Hz at 10 kHz offset from carrier. This model combines linear tuning with superior harmonic suppression. It provides a typical tuning sensitivity of 110 MHz/V and harmonic suppression better than –13 dBc while delivering an O/P power of 0 ±2.5 dBm over the extended operating temperature range of –40° to 85°C. Size: 0.50" × 0.50" × 0.22". Price: $18.95/VCO. Delivery: stock to four weeks.



Z-Communications Inc.,
San Diego, CA (858) 621-2700,
www.zcomm.com.

RS No. 225

New Products

Components

High Current Bias Tee

This 7/16 DIN bias tee is designed for wireless communication applications and operates in a frequency range from 500 MHz to 2.5 GHz with 7 amps DC current and 100 V DC voltage. There are a variety of connector options for the DC input. Typical insertion loss is 0.25 dB, 0.50 dB maximum while typical VSWR is 1.25, 1.50 maximum. The unit pictured is the model 8820D, and it is also available in a weatherproof version, model 8821D. Because of their rugged construction, both models are well suited for base station operations.

Aeroflex/Inmet,
Ann Arbor, MI (734) 426-5553,
www.aeroflex-inmet.com.

RS No. 226

Programmable Attenuator

The model M-DVAN-6018-60DD-SK is a programmable attenuator that incorporates a new linearization circuit to enable fast and accurate attenuation switching. The new design focuses on quick settling and stable operation over temperature extremes. Switching between any attenuation level is typically settled within 1 dB in about 400 ns. Temperature stability is ±1 dB over –10° to 85°C. The M-DVAN-6018-60DD-SK uses a hermetic MIL-C-28747 14 pin connector. Size: 1.34" × 1.34" × 0.5".

American Microwave Corp.,
Frederick, MD (301) 662-4700,
www.americanmicrowavecorp.com.

RS No. 227

High Power, Low Capacitance Resistors

From 20 to 250 W, this new resistor series is specifically designed to offer maximum power performance with low capacitance in power combiner and divider applications. These resistors are available in aluminum nitride and BeO. The resistors are offered as flange-mount, leaded chips, or as a surface-mount chip. When designing a Wilkinson power combiner or divider, this series eliminates the need to choose either high power or low capacitance because the resistors offer both.

Barry Industries,
Attleboro, MA (508) 226-3350,
www.barryind.com.

RS No. 229

Bias Tee

The SE bias tee 4-21 has been designed to provide DC power via the RF feeder coaxial cable. It is capable of supplying devices with DC power in the range of 24 to 72 VDC, with a maximum DC power of 12 A at 24 VDC. The SE bias tee 4-21 consists of two RF paths, one that can be switched on and off manually. It is used for coupling the DC voltage onto the coaxial cable and for separating the DC voltage from the RF signal. The bias tee exhibits low insertion loss over the applicable frequency ranges of 132 kHz, 10.7 MHz and 380 to 2170 MHz. It has dimensions of 68 by 229 by 94 mm, the RF connectors are of type 7/16 DIN and with ingress protection to IP65, the bias tee is capable of a wide range of applications, especially outdoors.

Andrew Wireless Systems GmbH,
Buchdorf, Germany +49 9099 69 151,
www.andrew.com.

RS No. 228

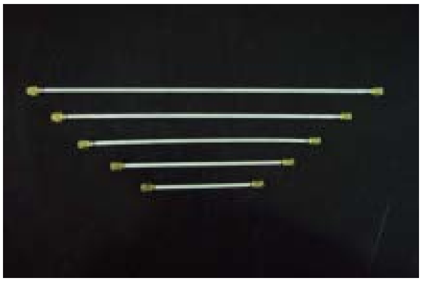
Non-blocking Matrix

The DK-PXI-1001 is a multi-functional radio frequency (RF) switching module designed for mobile, desktop testing stations. The matrix is compatible with a PXI standard chassis and cards. Originally configured as an 18 GHz, 4 × 4 non-blocking matrix, the new PXI card offers the flexibility and cost savings of multiple switching configurations in one unit. After the removal of six semi-rigid cables, the user has direct access to 12 internal ports allowing further standard or custom arrangements of the switching network.

Dow-Key Microwave Corp.,
Ventura, CA (805) 650-0260,
www.dowkey.com.

RS No. 230

Hand-formable Semi-rigid Assemblies



These semi-rigid assemblies (E Z Bend) are hand-formable during installation and feature low loss. The assemblies have been tested to 18 GHz and offer 100 percent RF shielding with copper or solderable aluminum outer conductor for 50 percent weight savings, sizes 0.086" and 0.141" diameter. The SMA style connectors offer guaranteed performance and eliminate costly drawings. Two inch to 18" straight lengths are available from stock for $10.00 each, 10 piece minimum. Other connector styles are available as well as longer lengths.
Haverhill Cable and Manufacturing Corp., Haverhill, MA (978) 372-6386, www.haverhillcable.com.

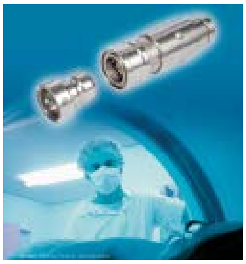
RS No. 231

SMT MMIC Mixers

Models HMC144LH5 and HMC338LC3B are GaAs MMIC mixers that are ideal for point-to-point and point-to-multipoint radios, VSAT, telecom, test instrumentation, radar, ECM and space applications from 6 to 34 GHz. The HMC144LH5 is a double-balanced MMIC mixer that can be used as an upconverter or downconverter from 6 to 20 GHz and requires no external components or DC biasing. The HMC338LC3B is a compact 24 to 34 GHz sub-harmonically pumped (×2) MMIC mixer with an integrated LO amplifier housed in a leadless RoHS compliant ceramic SMT package.
Hittite Microwave Corp., Chelmsford, MA (978) 250-3343, www.hittite.com.

RS No. 232

Medical RF Connectors



The MedLock RF coaxial connector series is designed for use in medical equipment and features an innovative quick-lock coupling mechanism. This coupling technology provides reliability and facilitates easy and fast mounting. The medical RF connectors are suitable for applications up to 5800 MHz. The service load at 2.4 GHz is 500 W and typical applications are in therapeutic devices like magnetic field therapies as well as RF controlled medical measurement and monitoring systems. The connectors have an extended connector housing, which provides strain relief and prevents bending and cable damage, ensuring good electrical performance throughout their lifetime.
IMS Connector Systems, Löffingen, Germany, +49 7654 901 401, www.imscs.com.

RS No. 233

Duplexer

The model WD-00069 is a duplexer that covers the full advanced wireless services (AWS) frequencies. The WD-00069 duplexer exhibits less than 0.5 dB of insertion loss across the passbands of 1710 to 1755 MHz and 2110 to 2155 MHz while providing greater than 80 dB of rejection. The unit measures 5.0" × 4.0" × 2.3" and is available from stock. Other mechanical configurations and weatherproofing options are available.
Lorch Microwave, Salisbury, MD (410) 860-5100, www.lorch.com.

RS No. 234

Isolators/Circulators

These connectorized isolators and circulators are designed for high frequency X- and Ku-band (8 to 18 GHz) applications that feature SMA-Female connectors and average power ratings of 2 W. Other specifications include 0.4 dB insertion loss, 1.30 VSWR and 18 dB isolation across the entire band. Units are available from stock to four weeks ARO. Made in the USA.

MECA Electronics, Denville, NJ (973) 625-0661, www.e-meca.com.

RS No. 248

DC Block

The model HR-25N is a low cost DC block for wireless coaxial cable feed applications. This model blocks the DC and low frequency current surges from passing on the inner conductor of a transmission line, while allowing unimpeded transmission of RF signals. RF loss is specified as below 0.08 dB over the frequency range from 380 to 2700 MHz. Common applications include blocking surges in subway tunnels and at wireless antenna sites. Units are RoHS compliant and sealed to IP65.
Microlab/FXR, Parsippany, NJ (973) 386-9696, www.microlab.fxr.com.

RS No. 235

High Power PIN Diodes

These non-magnetic metal electrode leadless faced (MELF) packaged PIN diodes feature high power handling and low distortion. These MELF PIN diodes are designed for switching and attenuator applications from HF through UHF frequencies. The diodes are manufactured using the company's propriety glassing process that features full-face bonding on the anode and cathode of the device to ensure full surface contact of the square ceramic package. This creates lower electrical and thermal resistance and provides higher average performance at RF power levels up to 100 W CW. The diodes also feature low series resistance that leads to low inductance characteristics, and low junction capacitance, which delivers high isolation.
MicroMetrics Inc., Londonderry, NH (603) 641-3800, www.micrometrics.com.

RS No. 236

Absorptive Bandstop Filter

These absorptive bandstop filters are designed for ruggedized high reliability applications. The filters operate in a frequency range from 10 to 1000 MHz and feature a tight shape factor notch of 1.44:1 and high operating power of 50 W. Custom designs and package options are available (BNC, GPO, GPPO and SMA interfaces).
Networks International Corp.,
Overland Park, KS (913) 685-3400,
www.nickc.com.

RS No. 238

Bias Tees and DC Blocks

In addition to the company's high frequency 40 GHz bias tees and DC blocks, MITEQ has now introduced a new line of low frequency, low cost bias tees and DC blocks. Frequency ranges start from 30 kHz to 20 GHz. Both have low insertion loss. Both connector (Size: 0.64" × 0.7" × 0.29") and surface-mount (Size: 0.69" × 0.60" × 0.18") versions are available. Options include different frequency bandwidths and various connector types.
MITEQ Inc.,
Hauppauge, NY (631) 436-7400,
www.miteq.com.

RS No. 249

Adapter/Attenuator

This line of adaptenuators is simply an attenuator with different type input and output connectors.

These adaptenuators feature improved interface matching and eliminate the hassle of working with, misplacing and stocking all different types of adapters to fit specific attenuators. These adaptenuators are designed with an ultra-wideband frequency response, usable to 4 GHz with a super flat frequency response. This line is durably built with solid unibody construction. Price: \$19.95 each (1–24). Delivery: in stock.
Mini-Circuits,
Brooklyn, NY (718) 934-4500,
www.minicircuits.com.

RS No. 237

GPS Notch Filter

The part number 9R7-1575.42-50S11 is a highly selective cavity notch filter. This unit is centered at the GPS frequency of 1575.42 MHz and offers a nominal 1 dB bandwidth of 50 MHz. The notch depth is greater than 70 dB at a center frequency of ±25 MHz and offers an insertion loss measuring less than 0.5 dB.
Reactel Inc.,
Gaithersburg, MD (301) 519-3660,
www.reactel.com.

RS No. 239

Two-way High Power Combiner

This two-way high power combiner is designed for the 800 and 900 MHz cellular band applications.

This combiner is aimed for providing a common antenna port for two different cellular networks that operate on different power levels. The combiner incorporates

a novel Wilkinson resistor arrangement coupled with a fan cooled, high efficiency heat sink that enables input power imbalance of up to 200 W between ports. For balanced signals on the input ports, this combiner can sustain power levels up to 1000 W composite per channel. Size: 5" × 5" × 4".
Renaissance Electronics Corp.,
Harvard, MA (978) 772-7774,
www.rec-usa.com.

RS No. 240

SMA Switch

The micro miniature SMA switch is a single-pole two position type. The switch incorporates SMA connectors to allow high density packaging and good electrical performance through 26.5 GHz. The switch is available in failsafe and latching configurations with a choice of three different frequency ranges and three different coil voltages.
RLC Electronics Inc.,
Mount Kisco, NY (914) 241-1334,
www.rlcelectronics.com.

RS No. 241

Extension Shaft

This extension shaft option is designed for multi-turn trimmer capacitors. Extension shafts can now be specified as short as 1/2" to over 40" or longer. Shorter length shafts will be metallic and longer lengths will be Delrin. Other materials may be specified per a customer's specific needs. Pricing for this extension shaft option based on its material is $40 each plus the cost of the capacitor. Delivery: four weeks.
Voltronics Corp.,
Denville, NJ (973) 586-8585,
www.voltronicscorp.com.

RS No. 243

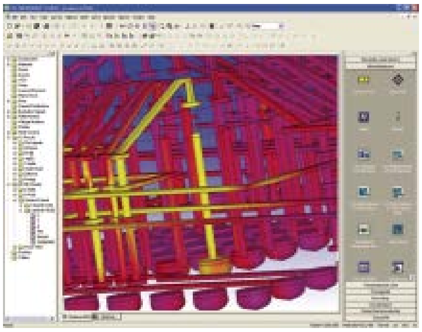
Coaxial Resonators

These ceramic coaxial resonators utilize a proprietary metallization process that provides excellent electrode adherence and superior Q. The resonators, which are built with rugged, thermally stable ceramics, are offered in three sizes and four dielectric constants with a frequency range from 800 MHz to 5.9 GHz. Typical applications for this product include voltage-controlled oscillators (VCO), bandpass filters and duplexers. Special features include excellent solderability, circuit miniaturization, high quality factor Q and repeatability of design.
Tusonix,
Tucson, AZ (520) 744-0400,
www.tusonix.com.

RS No. 242

SOFTWARE

EM Software Alternative



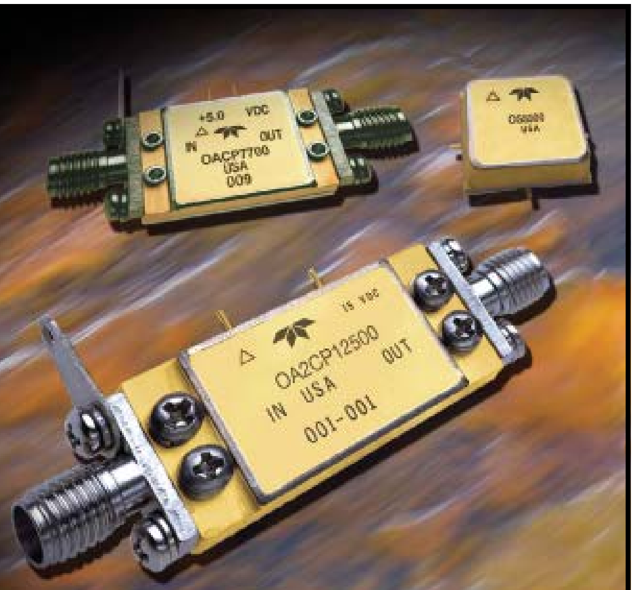
Newly introduced is the facility for users to run CST Studio Suite's™ EM simulation solvers on Red Hat Enterprise Linux version 3 or 4, as an alternative to Microsoft Windows versions. Alongside the five fully featured high frequency CST Microwave Studio® (MWS) solvers, the low frequency and static modules included in Studio Suite have been ported to Linux. In addition to Linux support, the MWS 2006B offers enhanced performance and robustness particularly in the Time Domain solver, thanks to the new Fast PBA mesher and flexible subgridding scheme with drastically reduced memory requirements. Also, users of the Frequency Domain solver now benefit from numerous new features and improvements such as the facility to excite structures by plane waves and slanted ports.
CST,
Darmstadt, Germany +49 (0) 6151 73030,
www.cst.com.

RS No. 245

Top Performers:

85 MHz to 18 GHz

VCOs



Teledyne Cougar's VCO circuits are designed for best overall phase noise and fastest settling time. Using silicon bipolar transistors and silicon varactor diodes make Cougar VCOs the smart choice for performance challenges.

Cougar's designs use a fundamental oscillator approach for the 85 MHz to 9 GHz VCOs and a doubling oscillator approach for the 9 GHz to 18 GHz VCOs.

Teledyne Cougar is your one-stop source for catalog and custom VCOs, RF and Microwave components, subsystems, and value-added service needs.

Model	Freq. Range (MHz)	Tuning Voltage Range (Volts)	Output Power/ Variation (dBm/ ±dB)	Typical Phase Noise Offset at 10kHz/100kHz (dBc/Hz)	Nominal Modulation Sensitivity Min.-Max. (MHz/V)	Typical Harmonic Suppression (dBc)	D.C. Bias Voltage (Volts)	D.C. Bias Current (mA)
Oscillator with internal MMIC amplifier available in SMTO-8 or CougarPak™								
OAS5100	4300-5100	0-15	13.0/2.0	-84/-108	50-85	-22	5.0	94
OAS7700	5700-7700	0-15	10.0/2.0	-75/-100	70-250	-30	5.0	95
OAS8900	6900-8900	0-15	10.0/2.0	-70/-95	100-270	-30	5.0	95
Oscillator available in SMTO-8 or CougarPak™								
OS6700	5400-6700	0-15	0/2.0	-75/-100	80-180	-17	5.0	25
OS7700	5700-7700	0-15	2.0/2.0	-75/-100	70-250	-17	5.0	25
OS8900	6900-8900	0-15	1.0/2.0	-70/-95	100-270	-25	5.0	24
Oscillator available in TO-8, SMTO-8 or CougarPak™								
OC150	85-150	0-20	10.0/2.0	-100/-120	2-8	-8	15.0	35
OC1850	1250-1850	0-15	8.0/2.0	-83/-111	20-70	-12	15.0	37
OC4500	3500-4500	0-15	8.0/2.0	-75/-100	50-150	-10	15.0	60
Oscillator, Amp, Filter and Voltage Regulator in 2- and 3-Stage CougarPak™								
OA2CP1001	500-1000	0-(-12)	15.0/2.0	-75/-105	30-60	-15	15.0	250
OA2CP12500	9000-12500	0-(-12)	15.0/2.0	-65/-95	150-450	-25	15.0	250
OA3CP18001	12000-18000	0-(-12)	15.0/2.0	-55/-85	150-750	-15	15.0	350

Typical and guaranteed specifications vary versus frequency; see detailed data sheets for specification variations.

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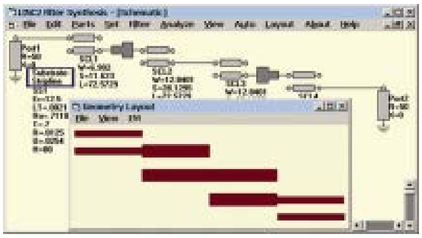
NEW PRODUCTS

Filter Synthesis Software



ACS has recently released a new version of its LINC2 filter synthesis software. LINC2 Filter Pro designs lumped and distributed filters in both single-ended and differential configurations. Version 1.13 adds DXF export capability to its layout viewer for transferring layout files to other programs. LINC2 DXF layout files can be translated to Gerber format for PCB fabrication. Microstrip and stripline filters can be analyzed with the built-in circuit simulator or exported to Sonnet's EM simulation program for electromagnetic simulation.

Applied Computational Sciences (ACS),
Escondido, CA
(760) 612-6988,
www.appliedmicrowave.com.

RS No. 244

TEST EQUIPMENT

VNA for mm-wave Testing

The Lightning Broadband ME7808C vector network analyzer has been enhanced to have high output power and improved calibration stability for accurate measurement of active and passive devices. Designed to address demanding mm-wave test applications, it can be configured for three completely independent configurations; 40 MHz to 110 GHz, 1 mm broadband coaxial systems, 65 GHz V-connector coaxial systems, and 65 GHz to 110 GHz extended W-band waveguide mm-wave systems. The system can also be upgraded to include a full range of banded mm-wave modules, which can be used to extend the frequency range beyond 110 GHz in standalone waveguide bands.

Anritsu EMEA Ltd.,
Luton, Bedfordshire, UK
+44 1582 433433,
www.anritsu.com.

RS No. 246

IEEE Radio & Wireless Symposium

22 - 24 January, 2008, Orlando, FL, USA

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Call For Papers

The 2008 IEEE Radio and Wireless Symposium (RWS 2008) incorporating IEEE Wireless and Microwave Technology Conference (WAMICON) will be held in Orlando, FL, on 22 - 24 January 2008 as part of the Radio Wireless Week technical event. In addition to oral presentations and posters, RWS 2008 includes workshops, panels, and an exhibition. Others collocating in the event are the Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF) and the IEEE Topical Workshop on Power Amplifiers for Wireless Communications (PA Symposium).

RWS 2008 sessions will highlight applications including (but not limited to):

- 3G/4G Wireless Communication including Emergency/Location Services
- Satellite Network and Wireless LAN Systems
- Software Defined Radio/Cognitive Radio and other Emerging Technologies
- 802.16/LMDS Broadband Fixed Wireless and Last-Mile Access Techniques
- Wireless Mesh and Broadband Local/Personal Area Networks
- Wireless Sensors and Ad Hoc Networks towards Anytime Anywhere Internetworking
- Ultrawideband (UWB) Technologies
- High-Power and Efficient RF Transmitters
- Low-Power/Low Noise RF/Analog IC and System-On-Chip Solutions
- Propagation, Channel Characterization and Fading Countermeasures
- Heterogeneous Mobile Networks and Mobile Network Convergence
- Wireless Security and RFID Technologies
- Seamless Mobility and All-IP Mobile Networks
- Multicasting and Broadcasting

Sessions will cover systems and enabling technologies in the areas of:

- Wireless System Architecture, Integration, and Convergence Issues
- Digital/Analog Adaptive/Collaborative Signal Processing
- System Level Design, Modeling, and Simulation
- MIMO/Space-Time Processing, Relaying Technology, and Smart Antennas
- Signal Generation/Power Amplification, Linearization, and Active Components
- Front-end Passive and Active Sub-systems
- Cross-Layer Design
- Radio on Fiber and optical techniques for UWB communications
- Electrically Small Antennas and handset Packaging

Workshop Proposals

Proposals for workshop topics are solicited, and must be received by 28 June 2007. Details on the process and requirements can be found at www.radiowireless.org.

Paper Submission Instructions

Authors must submit a summary (not more than 4 pages including figures) electronically using the www.radiowireless.org web page by **13 July 2007**; this is a firm date and will be strictly enforced! Authors can indicate their preference for oral or poster presentation format but the Technical Program Committee reserves the right regarding final presentation format decision. Please note that the only accepted file format is pdf.

Submissions will be evaluated for originality, significance of the work, technical content, and interest to a wide audience. Authors will be notified by 1 September 2007. Final manuscripts of accepted papers (4 pages in length) must be received by **4 November 2007** to be included in the published Proceedings.

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Design features should contain new and innovative technical ideas of practical use and interest to our predominantly engineering readers. Papers should be 14 to 16 double-spaced pages and contain 8 to 12 visual aids in the form of sketches, graphs, photographs or tables.

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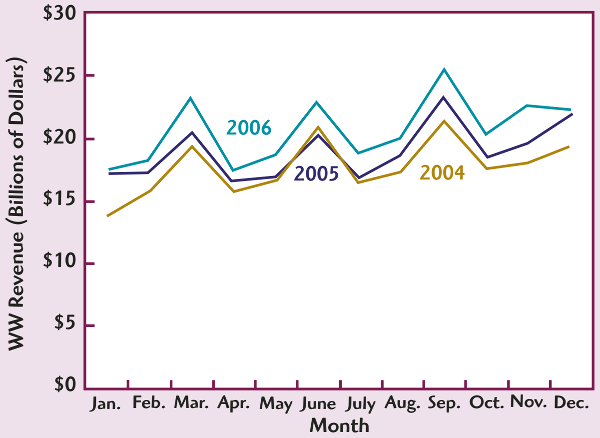
MICROWAVE METRICS

MONTHLY WORLDWIDE SEMICONDUCTOR REVENUE

The Semiconductor Industry Association (SIA) has released revenue numbers for December 2006 of $22.3 B (raw numbers not three-month moving average). The December numbers are up from $21.85 B in December of 2005 and represent a weak 2.1% growth month over month. Year-to-date growth for the full year ended at 8.5% down from 9.2% the prior month.

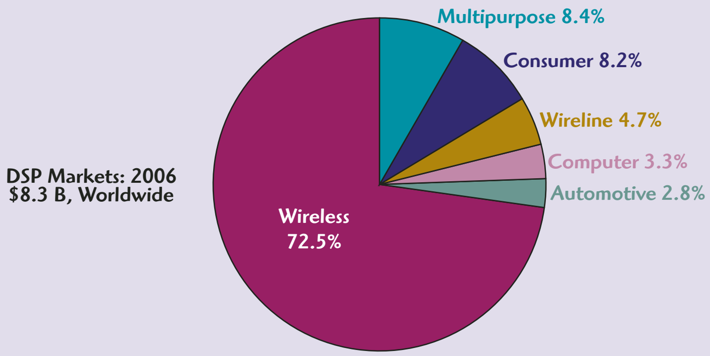
Notice how 2005 ran ahead of 2004 until May, took a three month pause and then began growing again. 2006 began the year even with 2005, then showed steady growth until December that once again ran even with 2005. December was a disappointing month and brought down the year-to-date average growth to 8.5% versus the expected 9% growth.



Source: IC Knowledge LLC, PO Box 20, Georgetown, MA 01833 (www.icknowledge.com)

2006 DSP CHIP REVENUE UP 9 PERCENT

DSP chip shipments rose to $8.3 B for calendar year 2006, a 9% increase over the prior year (and 1% under the forecast of 10%). This is slightly above the 8.7% growth of all monolithic integrated circuits. DSP shipments would have been higher if Q4 had at least been flat. Unfortunately, DSP shipments for the quarter were down 6.8% to the $2.01 B level, attributable mostly to a 6.5% drop in wireless. Consumer DSP shipments were up 10.3% while catalog and multipurpose DSP shipments were up 1.6%. The dramatic 60% quarterly drop in the relatively small "computer" segment is attributed to both inventory corrections and reclassification of disk drive controllers (to an "ASIC" category) in the PC market.



Source: Forward Concepts, 1575 W. University Dr., Suite III, Tempe, AZ 85281-3283 (www.fwdconcepts.com)

WIDEBAND

TRANSFORMERS

Model #	Z Ratio (50:Z)	Frequency (MHz)	Schematic
Wideband Series			
TM1-0	1:1	0.3 - 1000	1
TM1-1	1:1	0.4 - 500	2
TM1-2	1:1	50 - 1000	2
TM1-6	1:1	5 - 3000	5
TM1.5-2	1:1.5	0.5 - 550	1
TM2-1	1:2	1 - 600	2
TM4-0	1:4	0.2 - 350	2
TM4-1	1:4	10 - 1000	3
TM4-4	1:4	100 - 2500	3
TM2-GT	2:1	5 - 1500	4
TM4-GT	4:1	5 - 1000	4
TM8-GT	8:1	5 - 1000	4

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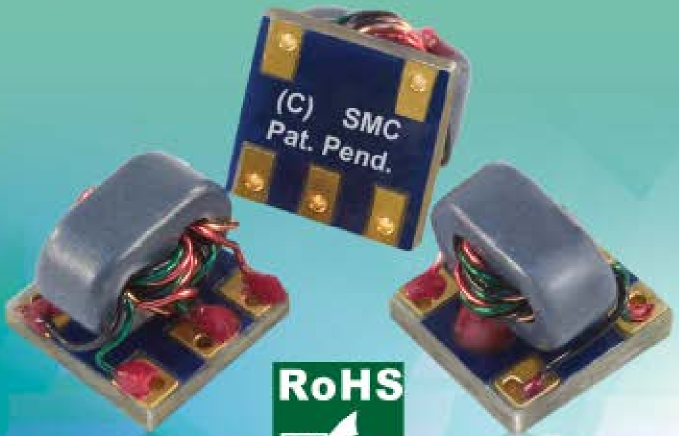
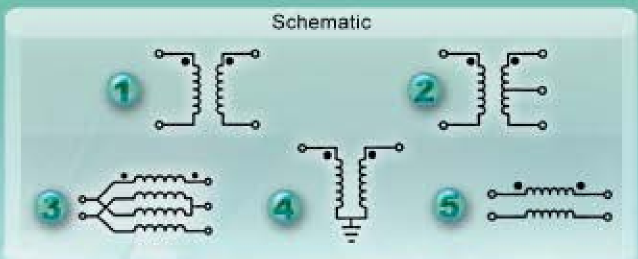
- > Low Cost
- > Wide Bandwidth
- > Good Amplitude / Phase Unbalance
- > Rugged Welded Construction
- > Lead Free RoHS Compliant
- > REL-PRO® Technology
- > Small Size, Surface Mount

Application:

- Impedance Matching
- Phase Shifting/Splitting
- Balance to Unbalance Transformation





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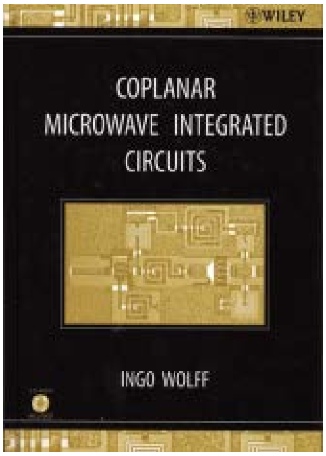
Coplanar Microwave Integrated Circuits



Ingo Wolff
Wiley Interscience • 557 pages; $120
ISBN: 0-471-12101-0

The subjects of this book—materials, technology, design and realization of coplanar microwave integrated circuits—combine the research results of a large research group under the leadership of the author. Chapter 1, the introduction, describes the different planar waveguides that can be used in planar microwave circuits, together with their properties, advantages and disadvantages. The full-wave propagation characteristics of coplanar waveguides are studied in Chapter 2, using rigorous analysis techniques such as the spectral domain analysis that is known to be a fast and accurate computation technique, especially well-suited for the analysis of planar transmission line structures. A first class of components that are of essential influence in the circuit design are the waveguide discontinuities, such as open and shorted ends, impedance steps, line gaps, waveguide bends, T-junctions and crossings. These elements are investigated in Chapter 3. One of the most important goals of microwave integrated circuits is the reduction of the needed space on the substrate material. Chapter 4 considers coplanar lumped elements, such as capacitors, inductors, transformers and resistors. Chapter 5 offers a coplanar element library and a circuit design program. Chapter 6 deals with coplanar filters and couplers. Whereas the previous chapters have been dealing with coplanar waveguides and components as well as coplanar techniques in general, Chapter 7 is dedicated to coplanar microwave integrated circuits. It starts with a short description of the active elements and their simulation background, after which design examples of coplanar switches, coplanar active filters and coplanar amplifiers are given. A coplanar electronic circulator and a special frequency doubler in coplanar technology are also shown.

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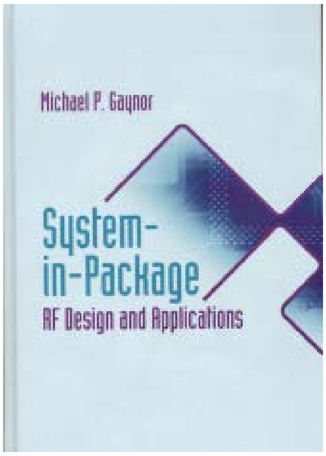
System-in-Package: RF Design and Applications



Michael P. Gaynor
Artech House • 234 pages; $99, £60
ISBN: 1-58053-905-X

The packaging industry has evolved recently from simple power amplifier modules to full dual-band cellular phone modules. The module advantages are size, cost, yield and ease of assembly. The system-in-package (SiP) designer has become a full RF transceiver designer, requiring complete RF knowledge of all the functional blocks of the transceiver as well as design for high volume manufacturing, reliability, shield requirements, substrate design rules, substrate performance and cost tradeoffs. The book starts with a brief history of the packaging industry, comparing system-on chip (SoC) to SiP, and concluding with the requirements for the SiP designer. Chapter 2 describes the various substrate options, with emphasis on the main substrates utilized in the low cost wireless module industry, LTCC and laminates. Chapter 3 is devoted to the assembly process, including process flow, component placement, solder paste and reflow, die attach, wirebonding, and die protection. Advanced packaging techniques are described in Chapter 4, including shielding and embedding passive components. SiP is no longer just a simple transistor package or PA module. Chapter 5 is dedicated to system architecture issues and concerns, while Chapter 6 offers RF design and simulation tips. Some advanced techniques for better RF performance and/or smaller size are given in Chapter 7. Chapter 8 describes a case study and offers thoughts on the field's future. A WLAN a/b/g complete RF transceiver module including a power amplifier has been designed with a two-compartment shield. The design process first reviewed all identifiable options to meet the design requirements without incurring new technology that would require qualifying in the assembly factory. Five options were identified and the size and cost of each are analyzed.

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ISO 9001 : 2000
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S5W2	S5W5	N5W5	5	±0.40
S6W2	S6W5	N6W5	6	±0.40
S7W2	S7W5	N7W5	7	-0.4, +0.9
S8W2	S8W5	N8W5	8	±0.60
S9W2	S9W5	N9W5	9	-0.4, +0.8
S10W2	S10W5	N10W5	10	±0.60
S12W2	S12W5	N12W5	12	±0.60
S15W2	S15W5	N15W5	15	±0.60
S20W2	S20W5	N20W5	20	-0.5, +0.8
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